Stratix IV GT 100G Development Kit

User Guide

101 Innovation Drive
San Jose, CA 95134
www.altera.com

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Contents

1. About This Kit

The Altera® Stratix® IV GT 100G Development Kit is a complete design environment that includes both the hardware and software you need to develop Stratix IV GT FPGA designs. The following list describes what you can accomplish with the kit:

- Test signal quality of the FPGA transceiver I/Os (up to 11.3 Gbps)
- Develop and test optical networking interfaces such as CFP, quad small-form-factor pluggable (QSFP), and small form-factor Pluggable (SFP+) interface
- Develop embedded designs utilizing the Nios® II processor and the SSRAM memory
- Develop and test network designs utilizing the Gigabit Ethernet PHY and the FPGA transceivers
- Develop FPGA designs for high-performance applications
- Measure the FPGA's power consumption

Kit Features

This section briefly describes the Stratix IV GT 100G Development Kit contents.

Hardware

The Stratix IV GT 100G Development Kit includes the following hardware:

- Stratix IV GT 100G development board—A development platform that allows you to develop and prototype hardware designs running on the Stratix IV GT EP4S100G5F45I1N FPGA.

  For detailed information about the board components and interfaces, refer to the *Stratix IV GT 100G Development Board Reference Manual*.

- Power supply and cables—The kit includes the following items:
  - Power supply and AC adapters for North America/Japan, Europe, and the United Kingdom
  - USB cable
  - Ethernet cable
  - CFP Loopback board with both passive and active retimed loopback features
  - QSFP loopback module
  - Two SFP+ loopback modules
  - Two Interlaken loopback boards

Software

The software for this kit, described in the following sections, is available on the Altera website for immediate downloading. You can also request to have Altera mail the software to you on DVDs.

Quartus II Subscription Edition Software

The Quartus II Subscription Edition Software is a licensed set of Altera tools with full functionality. Your kit includes a development kit edition (DKE) license for the Quartus II software (Windows platform only). This license entitles you to all the features of the subscription edition for a period of one year. After the year, you must purchase a renewal subscription to continue using the software. For more information, refer to the Altera website (www.altera.com).

Download the Quartus II Subscription Edition Software from the Quartus II Subscription Edition Software page of the Altera website. Alternatively, you can request a DVD from the Altera IP and Software DVD Request Form page of the Altera website.

The Quartus II Subscription Edition Software includes the following items:

- Quartus II Software—The Quartus II software, including the SOPC Builder system development tool, provides a comprehensive environment for system-on-a-programmable-chip (SOPC) design. The Quartus II software integrates into nearly any design environment and provides interfaces to industry-standard EDA tools.
- MegaCore® IP Library—A library that contains Altera IP MegaCore functions. You can evaluate MegaCore functions by using the OpenCore Plus feature to do the following:
  - Simulate behavior of a MegaCore function within your system
  - Verify functionality of your design, and quickly and easily evaluate its size and speed
  - Generate time-limited device programming files for designs that include MegaCore functions
  - Program a device and verify your design in hardware

  The OpenCore Plus hardware evaluation feature is an evaluation tool for prototyping only. You must purchase a license to use a MegaCore function in production.

  For more information about OpenCore Plus, refer to *AN 320: OpenCore Plus Evaluation of Megafunctions*.
- Nios® II Embedded Design Suite (EDS)—A full-featured set of tools that allow you to develop embedded software for the Nios II processor which you can include in your Altera FPGA designs.

Stratix IV GT 100G Development Kit Installer

The license-free Stratix IV GT 100G Development Kit installer includes all the documentation and design examples for the kit.

Download the Stratix IV GT 100G Development Kit installer from the Stratix IV GT 100G Development Kit page of the Altera website. Alternatively, you can request a development kit DVD from the Altera Kit Installations DVD Request Form page of the Altera website.

The remaining chapters in this user guide lead you through the following Stratix IV GT 100G development board setup steps:

- Inspecting the contents of the kit
- Installing the design and kit software
- Setting up, powering up, and verifying correct operation of the 100G development board
- Configuring the Stratix IV GT FPGA
- Running the Board Test System designs

For complete information about the 100G development board, refer to the *Stratix IV GT 100G Development Board Reference Manual*.

Before You Begin

Before using the kit or installing the software, check the kit contents and inspect the board to verify that you received all of the items listed in "Kit Features" on page 1–1. If any of the items are missing, contact Altera before you proceed.

Inspect the Board

To inspect board, perform the following steps:

1. Place the board on an anti-static surface and inspect it to ensure that it has not been damaged during shipment.

   CAUTION Without proper anti-static handling, you can damage the board.

2. Verify that all components are on the board and appear intact.

References

Use the following links to check the Altera website for other related information:

- For the latest board design files and reference designs, refer to the Stratix IV GT 100G Development Kit page.
- For the Stratix IV GT device documentation, refer to the Literature: Stratix IV Devices page.
- To purchase devices from the eStore, refer to the Devices page.
- For Stratix IV GT OrCAD symbols, refer to the Capture CIS Symbols page.
- For Nios II 32-bit embedded processor solutions, refer to the Embedded Processing page.

3. Software Installation

This chapter explains how to install the following software:

- Quartus II Subscription Edition Software
- Stratix IV GT 100G Development Kit
- USB-Blaster™ driver

Installing the Quartus II Subscription Edition Software

The Quartus II Subscription Edition Software provides the necessary tools for developing hardware and software for Altera FPGAs. Included in the Quartus II Subscription Edition Software are the Quartus II software, the Nios II EDS, and the MegaCore IP Library. The Quartus II software (including SOPC Builder) and the Nios II EDS are the primary FPGA development tools used to create the reference designs in this kit. To install the Altera development tools, perform the following steps:

1. Run the Quartus II Subscription Edition Software installer you acquired in "Software" on page 1–2.
2. Follow the on-screen instructions to complete the installation process.

If you have difficulty installing the Quartus II software, refer to *Altera Software Installation and Licensing*.

Licensing Considerations

Purchasing this kit entitles you to a one-year DKE license for the Quartus II Subscription Edition Software. Before using the Quartus II software, you must activate your license, identify specific users and computers, and obtain and install a license file.

If you already have a licensed version of the subscription edition, you can use that license file with this kit. If not, you need to obtain and install a license file. To begin, go to the Self Service Licensing Center page of the Altera website, log into or create your myAltera account, and take the following actions:

1. On the Activate Products page, enter the serial number provided with your development kit in the **License Activation Code** box.

   Your serial number is printed on the development kit box below the bottom bar code. The number is 10 or 11 alphanumeric characters and does not contain hyphens. Figure 3–1 shows the correct serial number as 3S150SPXXXX.

Figure 3–1. Locating Your Serial Number

2. Consult the Activate Products table, and to determine how to proceed, follow one of these steps:
   - If the administrator listed for your product is someone other than you, skip the remaining steps and contact your administrator to become a licensed user.
   - If the administrator listed for your product is you, proceed to step 3.
   - If the administrator listed for your product is *Stocking*, activate the product, making you the administrator, and proceed to step 3.
3. Use the Create New License page to license your product for a specific user (you) on specific computers. The Manage Computers and Manage Users pages allow you to add users and computers not already present in the licensing system.

   To license the Quartus II software, you need your computer's network interface card (NIC) ID, a number that uniquely identifies your computer. On the computer you use to run the Quartus II software, type `ipconfig /all` at a command prompt to determine the NIC ID. Your NIC ID is the 12-digit hexadecimal number on the **Physical Address** line.

4. When licensing is complete, Altera emails a **license.dat** file to you. Store the file on your computer and use the **License Setup** page of the **Options** dialog box in the Quartus II software to enable the software.

For complete licensing details, refer to *Altera Software Installation and Licensing*.

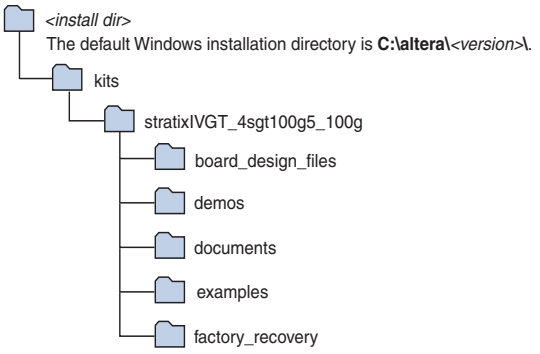
Installing the Stratix IV GT 100G Development Kit

To install the Stratix IV GT 100G Development Kit, perform the following steps:

1. Run the Stratix IV GT 100G Development Kit installer you acquired in "Software" on page 1–2.
2. Follow the on-screen instructions to complete the installation process. Be sure that the installation directory you specify is in the same relative location to your Quartus II software as the default locations.

The installation program creates the Stratix IV GT 100G Development Kit directory structure shown in Figure 3–2.

Figure 3–2. Stratix IV GT 100G Development Kit Installed Directory Structure *(1)*



Note to Figure 3–2:

(1) Early-release versions might have slightly different directory names.

Table 3–1 lists the file directory names and a description of their contents.

Table 3–1. Installed Directory Contents

Directory Name	Description of Contents
board_design_files	Contains schematic, layout, assembly, and bill of material board design files. Use these files as a starting point for a new prototype board design.
demos	Contains demonstration applications.
documents	Contains the kit documentation.
examples	Contains the sample design files for the Stratix IV GT 100G Development Kit.
factory_recovery	Contains the original data programmed onto the board before shipment. Use this data to restore the board with its original factory contents.

Installing the USB-Blaster Driver

The Stratix IV GT 100G development board includes integrated USB-Blaster circuitry for FPGA programming. However, for the host computer and board to communicate, you must install the USB-Blaster driver on the host computer.

Installation instructions for the USB-Blaster driver for your operating system are available on the Altera website. On the Altera Programming Cable Driver Information page of the Altera website, locate the table entry for your configuration and click the link to access the instructions.

4. Development Board Setup

This chapter explains how to set up the Stratix IV GT 100G development board.

Setting Up the Board

To prepare and apply power to the board, perform the following steps:

1. The Stratix IV GT 100G development board ships with its board switches preconfigured to support the design examples in the kit. If you suspect your board might not be configured with the default settings, follow the instructions in "Factory Default Switch Settings" on page 4–2 to return the board to its factory settings before proceeding.
2. Press FACTORY (S12) to load the Board Update Portal design from flash memory.
3. Connect the DC adapter (18.5 V, 120 W) to the DC power jack (J1) on the FPGA board and plug the cord into a power outlet.

   CAUTION: Use only the supplied power supply. Power regulation circuitry on the board can be damaged by power supplies with greater voltage.

4. Set the POWER switch (SW1) to the on position. When power is supplied to the board, a blue LED (D7) illuminates indicating that the board has power.

The MAX II device on the board contains (among other things) a parallel flash loader (PFL) megafunction. Pressing FACTORY (S12) configures the FPGA with the Board Update Portal from flash. Pressing PGM_SEL (S10) until POF 1 LED illuminates, and then pressing LOAD (S11) button configures the user hardware portion of flash memory.

The kit includes a MAX II design which contains the MAX II PFL megafunction. The design resides in the *<install dir>***kits\stratixIVGT_4sgt100g5_100g\examples\max2** directory.

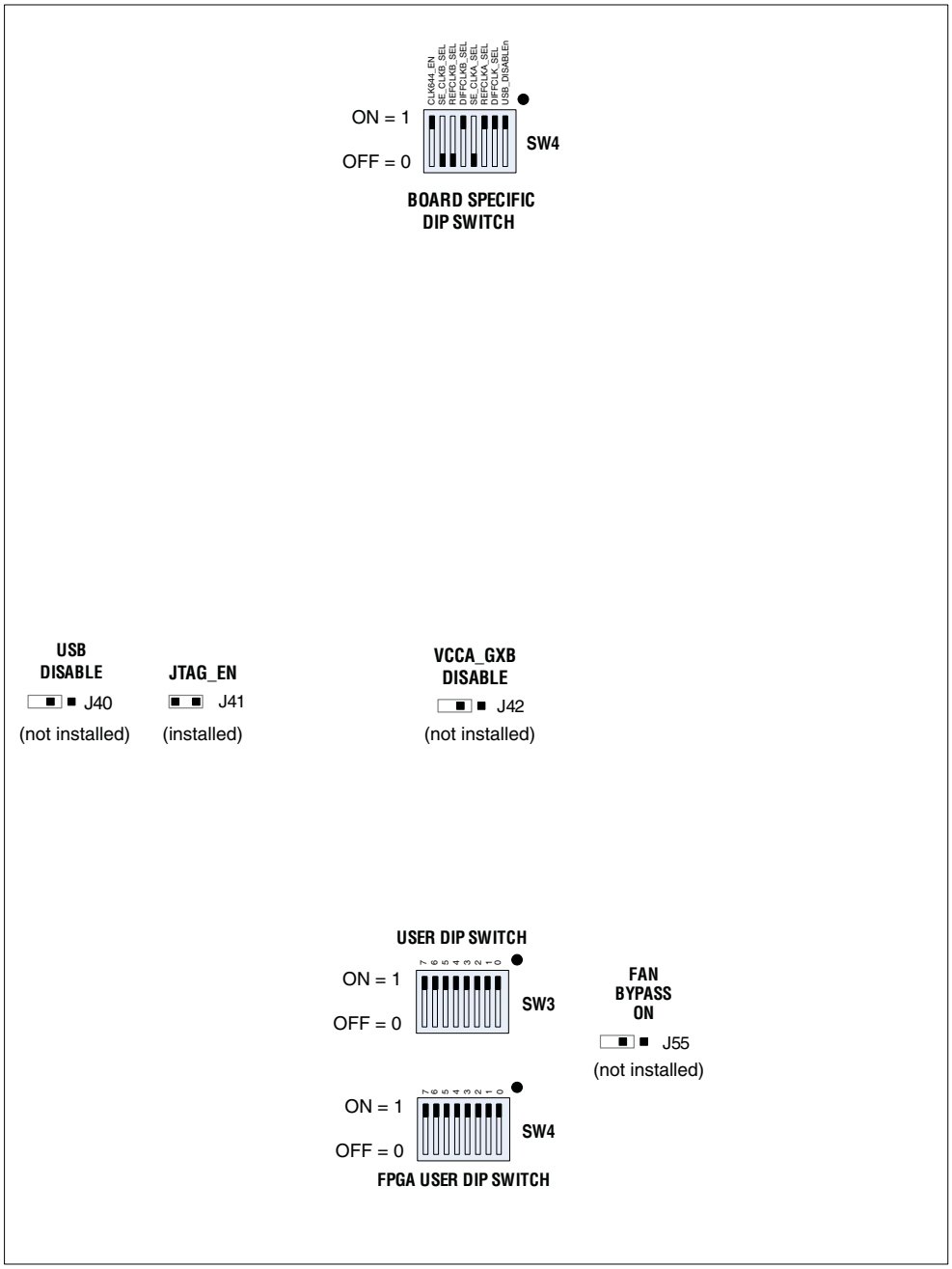
When configuration is complete, the MAX_CONF (D37) illuminates, signaling that you configured the Stratix IV GT device successfully.

For more information about the PFL megafunction, refer to *AN 386: Using the Parallel Flash Loader with the Quartus II Software*.

Factory Default Switch Settings

This section shows the factory switch settings for the Stratix IV GT 100G development board. Figure 4–1 shows the switch locations and the default position of each switch on the top side of the board.

Figure 4–1. Switch Locations and Default Settings on the Board Top



To restore the switches to their factory default settings, perform the following steps:

1. Set DIP switch bank (SW2) to match Table 4–1 and Figure 4–1.

2. Set the User DIP Switch bank (SW3) and FPGA User DIP Switch bank (SW4) to the 1 position, as shown in Figure 4–1.

Table 4–1. SW2 Dip Switch Settings

Switch	Board Label	Function	Default Position
1	USB_DISABLEn	Switch 1 has the following options: ■ When on, a logic 1 is selected. Enables the Embedded USB Blaster. ■ When off, a logic 0 is selected. Disables the Embedded USB Blaster.	On
2	DIFFCLKA_SEL	Switch 2 has the following options: ■ When on, a logic 1 is selected. The PLL for the single ended clock goes to the global clock inputs of the A tree structure. ■ When off, a logic 0 is selected. The SMA input for the single ended clock goes to the global clock inputs of the A tree structure.	On
3	REFCLKA_SEL	Switch 3 has the following options: ■ When on, a logic 1 is selected. The PLL goes to the transceivers on the A clock tree structure. ■ When off, a logic 0 is selected. The SMA input goes to the transceivers on the A clock tree structure.	On
4	SE_CLKA_SEL	Switch 4 has the following options: ■ When on, a logic 1 is selected. The SMA for the single ended clock goes to the global clock inputs of the A tree structure. ■ When off, a logic 0 is selected. The PLL for the single ended clock goes to the global clock inputs of the A tree structure.	Off
5	DIFFCLKB_SEL	Switch 5 has the following options: ■ When on, a logic 1 is selected. The PLL for the single ended clock goes to the global clock inputs of the B tree structure. ■ When on, a logic 1 is selected. The PLL for the single ended clock goes to the global clock inputs of the B tree structure.	On
6	REFCLKB_SEL	Switch 6 has the following options: ■ When off, a logic 0 is selected. The PLL goes to the transceivers on the B clock tree structure. ■ When on, a logic 1 is selected. The SMA goes to the transceivers on the B clock tree structure.	Off
7	SE_CLKB_SEL	Switch 7 has the following options: ■ When on, a logic 1 is selected. The SMA for the single ended clock goes to the global clock inputs of the B tree structure. ■ When off, a logic 0 is selected. The PLL for the single ended clock goes to the global clock inputs of the B tree structure.	Off
8	CLK644_EN	Switch 8 has the following options: ■ When on, a logic 1 is selected. Enables the 644.53125MHz clock. ■ When off, a logic 0 is selected. Disables the 644.53125MHz clock.	On

3. Set the board jumpers to match Table 4–2, as shown in Figure 4–1.

Table 4–2. Jumper Settings

Board Reference	Name	Default Shunt Position
J40	USB DISABLE	Not Installed
J41	JTAG_EN	Installed
J42	VCCA_GXB DISABLE	Not Installed
J55	FAN BYPASS ON	Not Installed

For more information about the FPGA board settings, refer to the *Stratix IV GT 100G Development Board Reference Manual*.

5. Board Update Portal

The Stratix IV GT 100G Development Kit ships with the Board Update Portal design example stored in the factory portion of the flash memory on the board. The design consists of a Nios II embedded processor, an Ethernet MAC, and an HTML web server.

Pressing FACTORY (S12) configures the FPGA with the Board Update Portal design example from flash memory. The design can obtain an IP address from any DHCP server and serve a web page from the flash on your board to any host computer on the same network. The web page allows you to upload new FPGA designs to the user hardware portion of flash memory, and provides links to useful information on the Altera website, including kit-specific links and design resources.

After successfully updating the user hardware flash memory, you can load the user design from flash memory into the FPGA. To do so, press PGM_SEL (S10) until the POF 1 LED illuminates, and then press LOAD (S11) to configure the user hardware portion of flash memory.

The source code for the Board Update Portal design resides in the *<install dir>***kits\stratixIVGT_4sgt100g5_100g\examples** directory. If the Board Update Portal is corrupted or deleted from the flash memory, refer to "Restoring the Flash Device to the Factory Settings" on page A–4 to restore the board with its original factory contents.

Connecting to the Board Update Portal Web Page

This section provides instructions to connect to the Board Update Portal web page.

Before you proceed, ensure that you have the following:

- A PC with a connection to a working Ethernet port on a DHCP enabled network.
- A separate working Ethernet port connected to the same network for the board.
- The Ethernet and power cables that are included in the kit.

To connect to the Board Update Portal web page, perform the following steps:

1. With the board powered down, attach the Ethernet cable from the board to your LAN.
2. Power up the board. The board connects to the LAN's gateway router, and obtains an IP address. The LCD on the board displays the IP address.
3. Launch a web browser on a PC that is connected to the same network, and enter the IP address from the LCD into the browser address bar. The Board Update Portal web page appears in the browser.
4. Click Stratix IV GT 100G Development Kit on the Board Update Portal web page to access the kit's home page. Visit this page occasionally for documentation updates and additional new designs.

You can also navigate directly to the Stratix IV GT 100G Development Kit page of the Altera website to determine if you have the latest kit software.

Using the Board Update Portal to Update User Designs

The Board Update Portal allows you to write new designs to the user hardware portion of flash memory. Designs must be in the Nios II Flash Programmer File (**.flash**) format.

Design files available from the Stratix IV GT 100G Development Kit page of the Altera website include **.flash** files. You can also create **.flash** files from your own custom design. Refer to "Preparing Design Files for Flash Programming" on page A–2 for information about preparing your own design for upload.

To upload a design over the network into the user portion of flash memory on your board, perform the following steps:

1. Perform the steps in "Connecting to the Board Update Portal Web Page" to access the Board Update Portal web page.
2. In the **Hardware File Name** field specify the **.flash** file that you either downloaded from the Altera website or created on your own. If there is a software component to the design, specify it in the same manner using the **Software File Name** field, otherwise leave the **Software File Name** field blank.
3. Click **Upload**.
4. To configure the FPGA with the new design after the flash memory upload process is complete, press PGM_SEL (S10) until the POF 1 LED illuminates, and then press LOAD (S11) to configure the user hardware portion of flash memory.

As long as you don't overwrite the factory image in the flash memory device, you can continue to use the Board Update Portal to write new designs to the user hardware portion of flash memory. If you do overwrite the factory image, you can restore it by following the instructions in "Restoring the Flash Device to the Factory Settings" on page A–4.

6. Board Test System

The kit includes a design example and application called the Board Test System to test the functionality of the Stratix IV GT 100G development board. The application provides an easy-to-use interface to alter functional settings and observe the results. You can use the application to test board components, modify functional parameters, observe performance, and measure power usage. The application is also useful as a reference for designing systems. To install the application, follow the steps in "Installing the Stratix IV GT 100G Development Kit" on page 3–2.

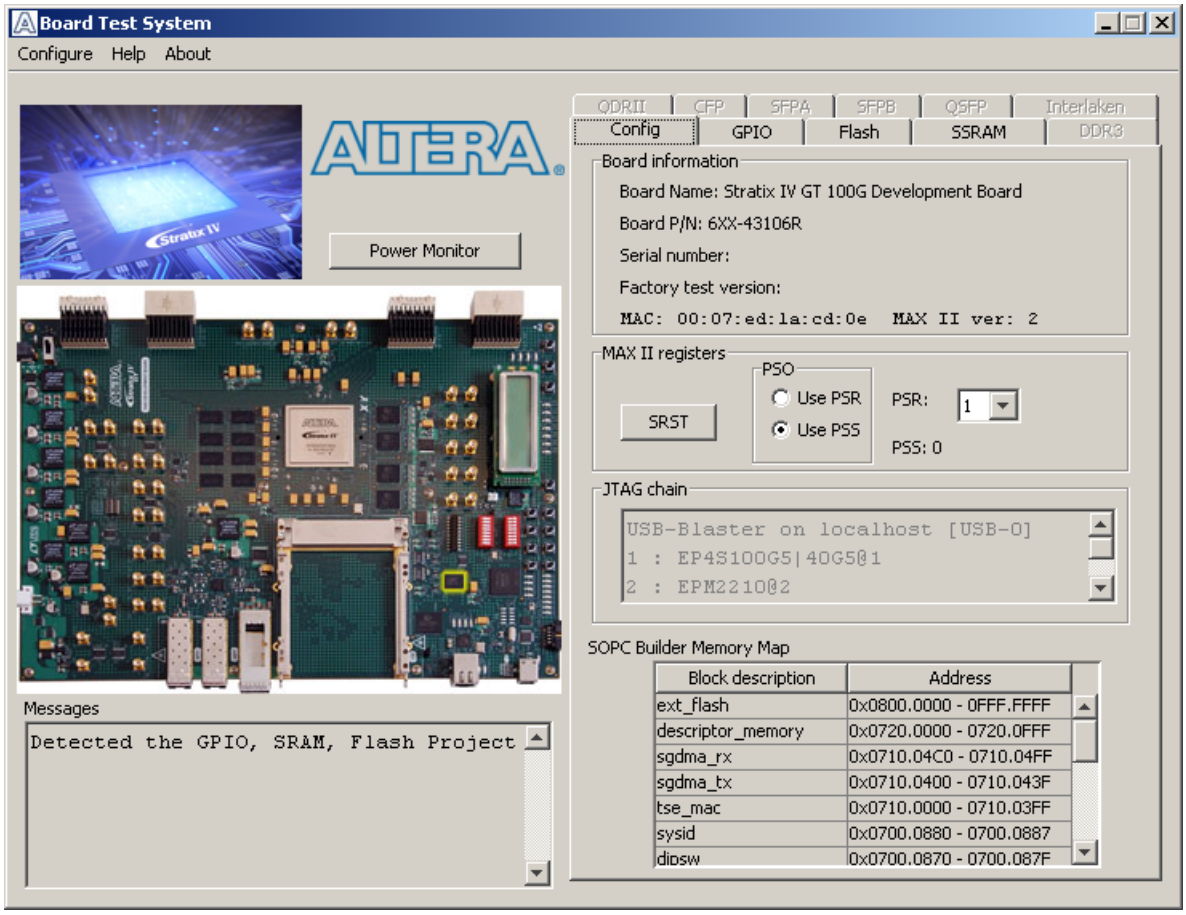
The application provides access to the following Stratix IV GT 100G development board features:

- General purpose I/O (GPIO)
- SRAM
- Flash memory
- Interlaken interfaces
- CFP loopback card
- QSFP optical networking module
- SFP+ optical networking modules
- QDR II SRAM interfaces
- DDR3 SDRAM interfaces

The application allows you to exercise most of the board components. While using the application, you reconfigure the FPGA several times with test designs specific to the functionality you are testing.

A GUI runs on the PC which communicates over the JTAG bus to a test design running in the Stratix IV GT device. Figure 6–1 shows the initial GUI for a board that is in the factory configuration.

Figure 6–1. Board Test System Graphical User Interface



Several designs are provided to test the major board features. Each design provides data for one or more tabs in the application. The Configure menu identifies the appropriate design to download to the FPGA for each tab.

After successful FPGA configuration, the appropriate tab appears and allows you to exercise the related board features. Highlights appear in the board picture around the corresponding components.

The **Power Monitor** button starts the Power Monitor application that measures and reports current power information for the board. Because the application communicates over the JTAG bus to the MAX II device, you can measure the power of any design in the FPGA, including your own designs.

The Board Test System and Power Monitor share the JTAG bus with other applications like the Nios II debugger and the SignalTap® II Embedded Logic Analyzer. Because the Quartus II Programmer uses most of the bandwidth of the JTAG bus, other applications using the JTAG bus might time out. Be sure to close the other applications before attempting to reconfigure the FPGA using the Quartus II Programmer.

Preparing the Board

With the power to the board off, perform the following steps:

1. Connect the USB cable to the board.
2. Verify the settings for the board settings DIP switches SW2, SW3, and SW4 match Figure 4–1 on page 4–2.

   For more information about the board's DIP switch and jumper settings, refer to the *Stratix IV GT 100G Development Board Reference Manual*.

3. Turn the power to the board on.
4. Press PGM_SEL (S10) until the POF 1 LED illuminates, and then press LOAD (S11) to configure the user hardware portion of flash memory.

   CAUTION

   To ensure operating stability, keep the USB cable connected and the board powered on when running the demonstration application. The application cannot run correctly unless the USB cable is attached and the board is on.

Running the Board Test System

To run the application, navigate to the *<install dir>***kits\stratixIVGT_4sgt100g5_100g\examples\board_test_system** directory and run the **BoardTestSystem.exe** application.

On Windows, click **Start** > **All Programs** > **Altera** > **Stratix IV GT 100G Development Kit** *<version>* > **Board Test System** to run the application.

A GUI appears, displaying the application tab that corresponds to the design running in the FPGA. The Stratix IV GT 100G development board's flash memory ships preconfigured with the design that corresponds to the test tabs.

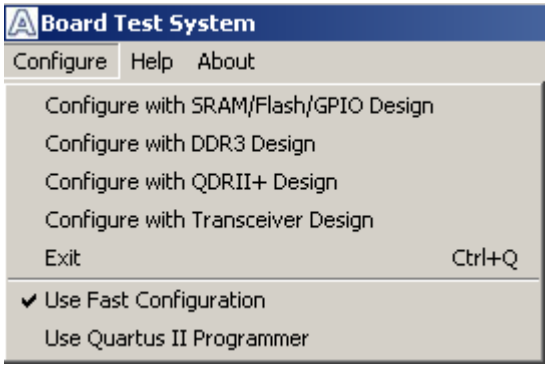
Using the Board Test System

This section describes each control in the Board Test System application.

The Configure Menu

Each test design tests different functionality and corresponds to one or more application tabs. Use the Configure menu to select the design you want to use. Figure 6–2 shows the Configure menu.

Figure 6–2. The Configure Menu



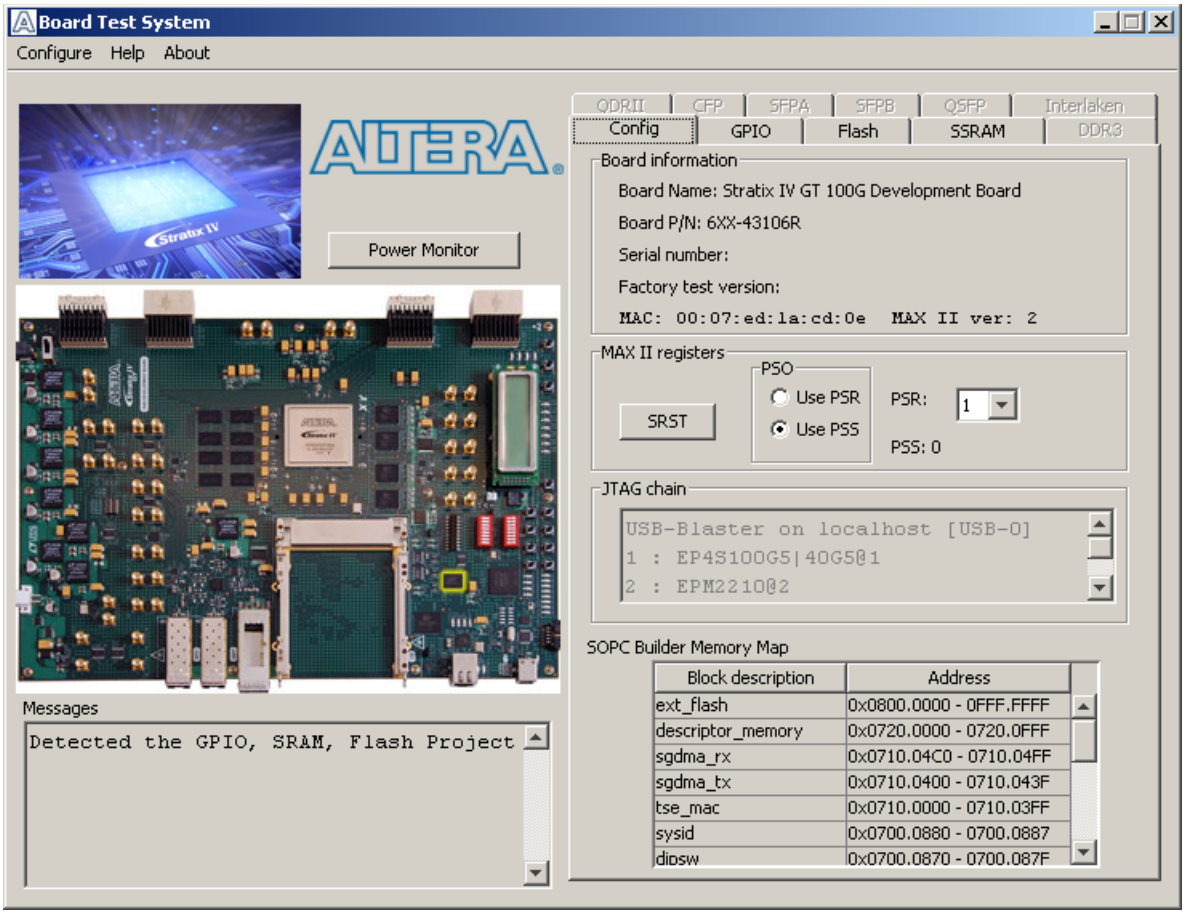
To configure the FPGA with a test system design, perform the following steps:

1. On the Configure menu, click one of the following options to determine how to pass data through the JTAG chain:
   - **Use Fast Configuration**—Compresses the data for faster loading.
   - **Use Quartus II Programmer**—Uses the standard JTAG-based configuration method.
2. On the Configure menu, click the configure command that corresponds to the functionality you wish to test.

The Config Tab

The **Config** tab shows configuration information for the 100G development board. Figure 6–3 shows the **Config** tab.

Figure 6–3. The Config Tab



The following sections describe the controls on the **Config** tab.

Board Information

The **Board information** controls display static information about your board.

- **Name**—Indicates the official name of the board, given by the Board Test System.
- **Part number**—Indicates the part number of the board.
- **Serial number**—Indicates the serial number of the board.
- **Factory test version**—Indicates the version of the Board Test System currently running on the board.
- **MAC**—Indicates the MAC address of the board.

- **MAX II ver**—Indicates the version of MAX II code currently running on the board. The MAX II code resides in the *<install dir>***kits\stratixIVGT_4sgt100g5_100g\examples** directory. Newer revisions of this code might be available on the Stratix IV GT 100G Development Kit page of the Altera website.

MAX II Registers

The **MAX II registers** control allow you to view and change the current MAX II register values as described in Table 6–1. Changes to the register values with the GUI take effect immediately. For example, writing a 0 to SRST resets the board.

Table 6–1. MAX II Registers

Register Name	Read/Write Capability	Description
System Reset (SRST)	Write only	Set to 0 to initiate an FPGA reconfiguration.
Page Select Register (PSR)	Read / Write	Determines which of the pages of flash memory to use for FPGA reconfiguration. The flash memory ships with pages 0 and 1 preconfigured.
Page Select Override (PSO)	Read / Write	When set to 0, the value in PSR determines the page of flash memory to use for FPGA reconfiguration. When set to 1, the value in PSS determines the page of flash memory to use for FPGA reconfiguration.
Page Select Switch (PSS)	Read only	Holds the current value of the illuminated USER_POF LED (D19, D20, D25) based on the following encoding: ■ 0 = USER_POF1 LED (D19) ■ 1 = USER_POF2 LED (D20) ■ 2 = USER_POF3 LED (D25)

- **PSO**—Sets the MAX II PSO register. The following options are available:
  - **Use PSR**—Allows the PSR to determine the page of flash memory to use for FPGA reconfiguration.
  - **Use PSS**—Allows the PSS to determine the page of flash memory to use for FPGA reconfiguration.
- **PSR**—Sets the MAX II PSR register. The numerical values in the list corresponds to the page of flash memory to load during FPGA reconfiguration. Refer to Table 6–1 for more information.
- **PSS**—Displays the MAX II PSS register value. Refer to Table 6–1 for the list of available options.
- **SRST**—Resets the system and reloads the FPGA with a design from flash memory based on the other MAX II register values. Refer to Table 6–1 for more information.

Because the **Config** tab requires that a specific design is running in the FPGA at a specific clock speed, writing a 0 to SRST or changing the PSO value can cause the Board Test System to stop running.

JTAG Chain

The **JTAG chain** control shows all the devices currently in the JTAG chain. The Stratix IV GT device is always the first device in the chain.

☞ The installed jumper for JTAG_EN (J41) includes the MAX II device in the JTAG chain.

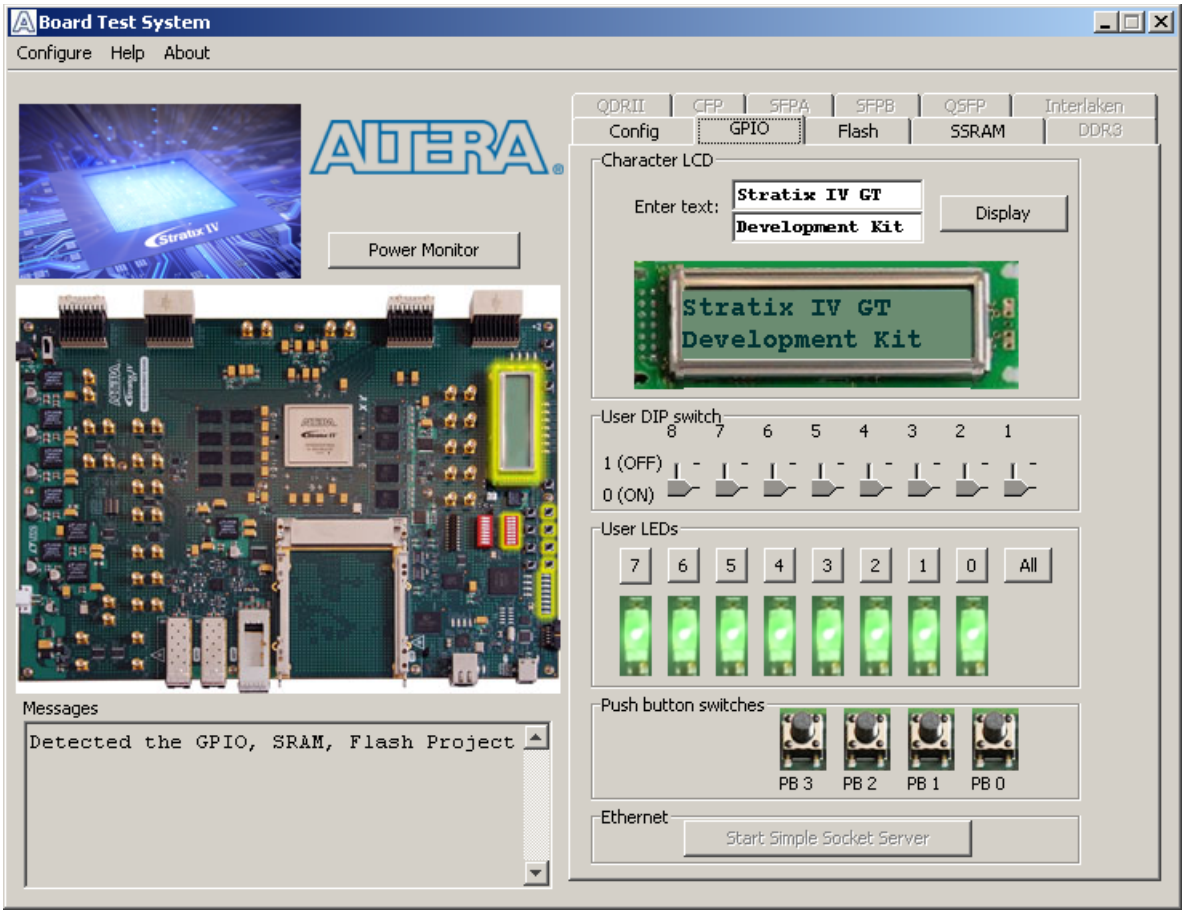
SOPC Builder Memory Map

Static display

The GPIO Tab

The **GPIO** tab allows you to interact with all the general purpose user I/O components on your board. Figure 6–4 shows the **GPIO** tab.

Figure 6–4. The GPIO Tab



The following sections describe the controls on the **GPIO** tab.

Character LCD

The **Character LCD** controls allow you to display text strings on the character LCD on your board. Type text in the text boxes and then click **Display**.

If you exceed the 16 character display limit on either line, a warning message appears.

User DIP Switches

The read-only **User DIP switches** control displays the current positions of the switches in the user DIP switch bank SW4. Change the switches on the board to see the graphical display change accordingly.

User LEDs

The **User LEDs** control displays the current state of the user LEDs. **Toggle LEDs** buttons to turn the board LEDs on and off.

Push Button Switches

The read-only **Push button switches** control displays the current state of the board user push buttons. Press a push button on the board to see the graphical display change accordingly.

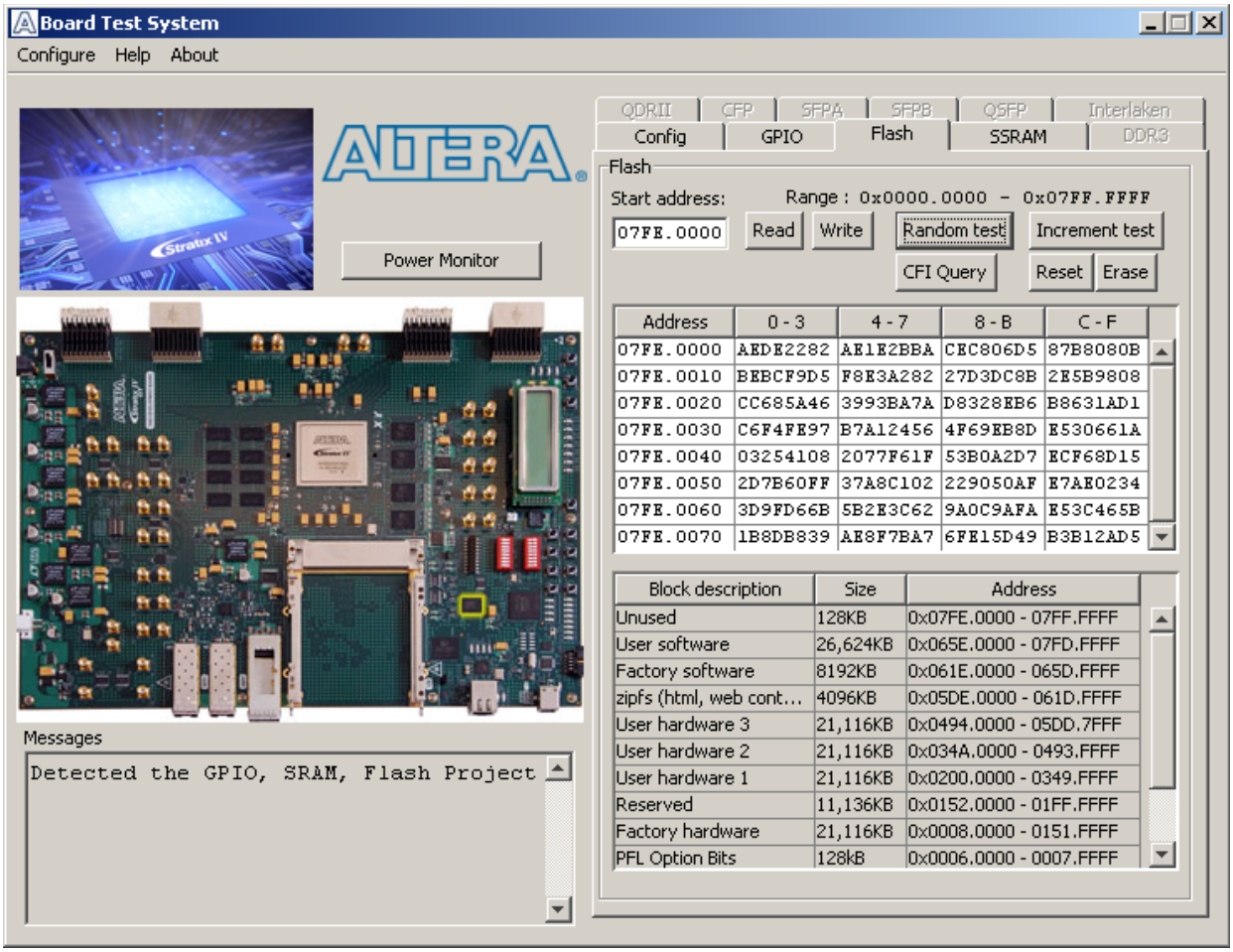
Ethernet

Click **Start Simple Socket Server** to run the **simple_socket_server.elf** program that was downloaded into FPGA during configuration.

The Flash Tab

The **Flash** tab allows you to read and write flash memory on your board. Figure 6–5 shows the **Flash** tab.

Figure 6–5. The Flash Tab



The following sections describe the controls on the **Flash** tab.

Read

The **Read** control reads the flash memory on your board. To see the flash memory contents, type a starting address in the text box and click **Read**. Values starting at the specified address appear in the table. The flash memory addresses display in the format the Nios II processor within the FPGA uses, that is, each flash memory address is offset by 0x08000000. Thus, the first location in flash memory appears as 0x08000000 in the GUI.

If you enter an address outside of 0xFDFFFFF to 0x0FFFFFFF flash memory address space, a warning message identifies the valid flash memory address range.

Write

The **Write** control writes the flash memory on your board. To update the flash memory contents, change values in the table and click **Write**. The application writes the new values to flash memory and then reads the values back to guarantee that the graphical display accurately reflects the memory contents.

To prevent overwriting the dedicated portions of flash memory, the application limits the writable flash memory address range to 0x08FE0000 to 0x08FFFFFF (which corresponds to address range 0x00FE0000 - 0x00FFFFFF in the uppermost portion of the user software memory block, as shown in Figure 6–1 on page 6–2 and Table A–1 on page A–1).

Random Test

Starts a random data pattern test to flash memory. Limited to scratch page upper 128K blocks.

CFI Query

The **CFI Query** control updates the memory table, displaying the CFI ROM table contents from the flash device.

Increment Test

Starts an incrementing data pattern test to flash memory. Limited to scratch page upper 128K blocks.

Reset

The **Reset** control executes the flash device's reset command and updates the memory table displayed on the **Flash** tab.

Erase

Erases flash memory. Limited to scratch page upper 128K blocks.

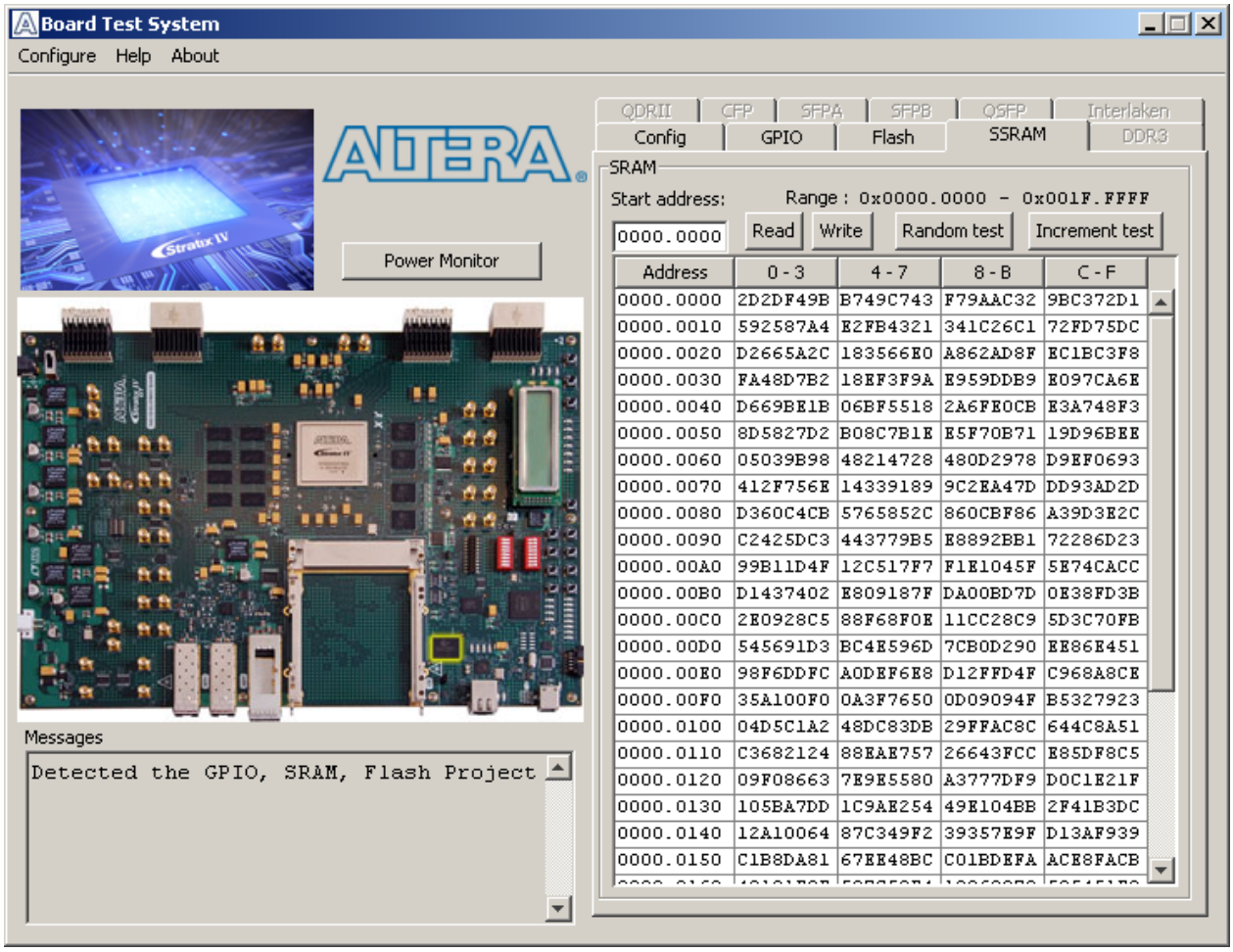
Flash Memory Map

Displays the flash memory map for the Stratix IV GT 100G Development Kit.

The SSRAM Tab

The **SSRAM** tab allows you to read and write SRAM and flash memory on your board. Figure 6–6 shows the **SSRAM** tab.

Figure 6–6. The SSRAM Tab



The following sections describe the controls on the **SSRAM** tab.

Read

The **Read** control reads the SSRAM on your board. To see the SSRAM contents, type a starting address in the text box and click **Read**. Values starting at the specified address appear in the table. The SSRAM addresses display in the format the Nios II processor within the FPGA uses, that is, each SSRAM address is offset by 0x00200000. Thus, the first location in SSRAM appears as 0x00200000 in the GUI.

If you enter an address outside of the 0x00200000 to 0x003FFFFF SSRAM address space, a warning message identifies the valid SSRAM address range.

Write

The **Write** control writes the SSRAM on your board. To update the SSRAM contents, change values in the table and click **Write**. The application writes the new values to SSRAM and then reads the values back to guarantee that the graphical display accurately reflects the memory contents.

Random Test

Starts an random data pattern test to flash memory. Limited to scratch page upper 128K blocks.

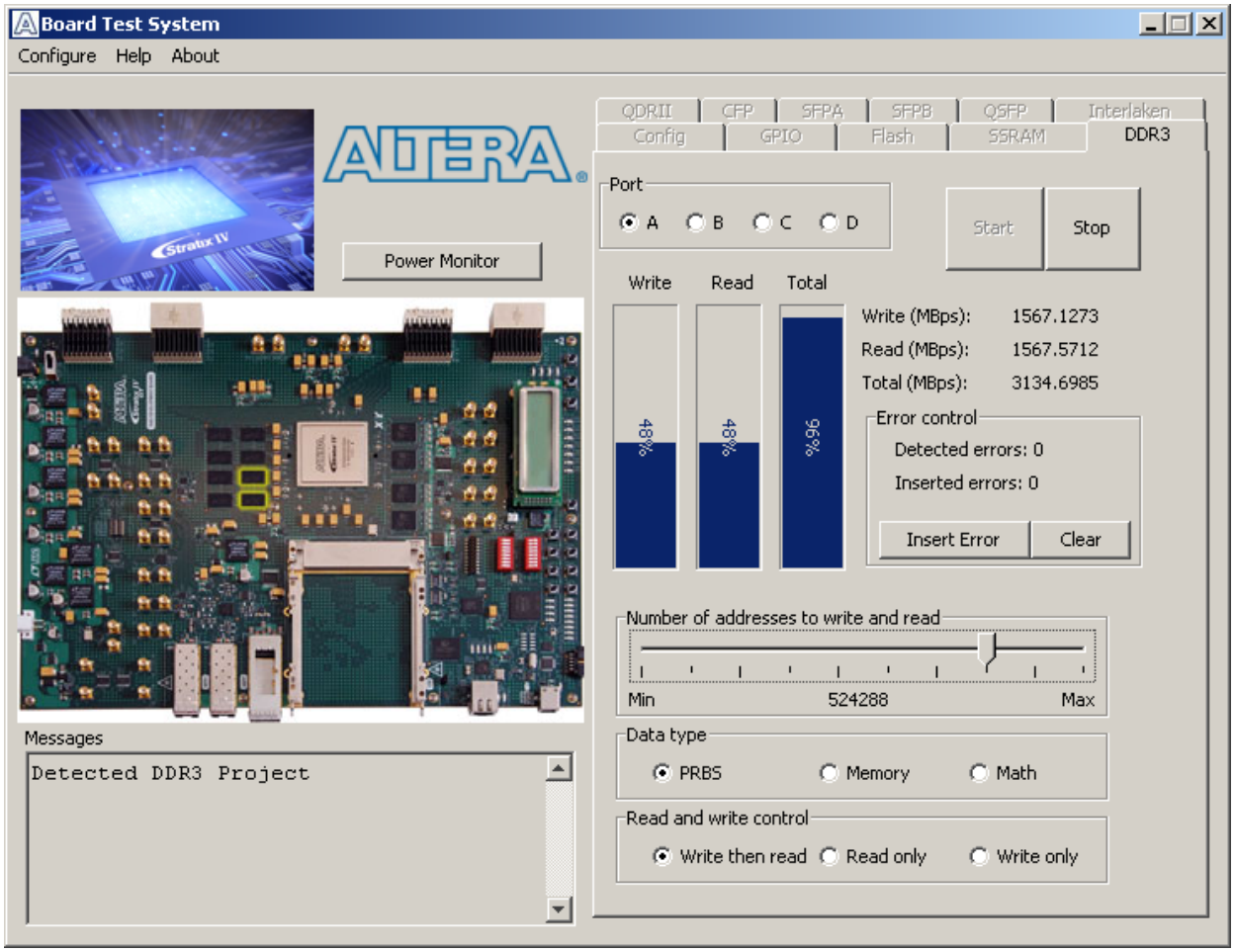
Incrementing Test

Starts an incrementing data pattern test to flash memory. Limited to scratch page upper 128K blocks.

The DDR3 Tab

The **DDR3** tab allows you to independently test each of the DDR3 memory interfaces on your board. Figure 6–7 shows the **DDR3** tab. Since there are four DDR3 ports on the Stratix IV GT 100G board, the DDR3 tab has 4 radio buttons to monitor each DDR3 interface.

Figure 6–7. The DDR3 Tab



The following sections describe the controls on the **DDR3** tab.

Port

This control directs communications to one of four DDR3 memory ports on the board. Each interface is 32 bits wide.

Start

The **Start** control initiates DDR3 memory transaction performance analysis.

Stop

The **Stop** control terminates transaction performance analysis.

Performance Indicators

These controls display current transaction performance analysis information collected since you last pressed **Start**:

- **Write**, **Read**, and **Total** performance bars—Show the percentage of maximum theoretical data rate that the requested transactions are able to achieve.
- **Write (MBps)**, **Read (MBps)**, and **Total (MBps)**—Show the number of bytes of data analyzed per second. Each DDR3 port is 32 bits wide and the frequency is 400 MHz double data rate (800 Mbps per pin), equating to a theoretical maximum bandwidth of 3200 MBps.

Error Control

The **Error control** controls display data errors detected during analysis and allow you to insert errors:

- **Detected errors**—Displays the number of data errors detected in the hardware.
- **Inserted errors**—Displays the number of errors inserted into the transaction stream.
- **Insert Error**—Inserts a one-word error into the transaction stream each time you click the button. **Insert Error** is only enabled during transaction performance analysis.
- **Clear**—Resets the **Detected errors** and **Inserted errors** counters to zeros.

Number of Addresses to Write and Read

The **Number of addresses to write and read** control determines the number of addresses to use in each iteration of reads and writes. Valid values range from 8 to 131072.

Data Type

The **Data type** control specifies the type of data contained in the transactions. The following data types are available for analysis:

- **PRBS**—Selects pseudo-random bit sequences.
- **Memory**—Selects a generic data pattern stored in the on chip memory of the Stratix IV GT device.
- **Math**—Selects data generated from a simple math function within the FPGA fabric.

Read and Write Control

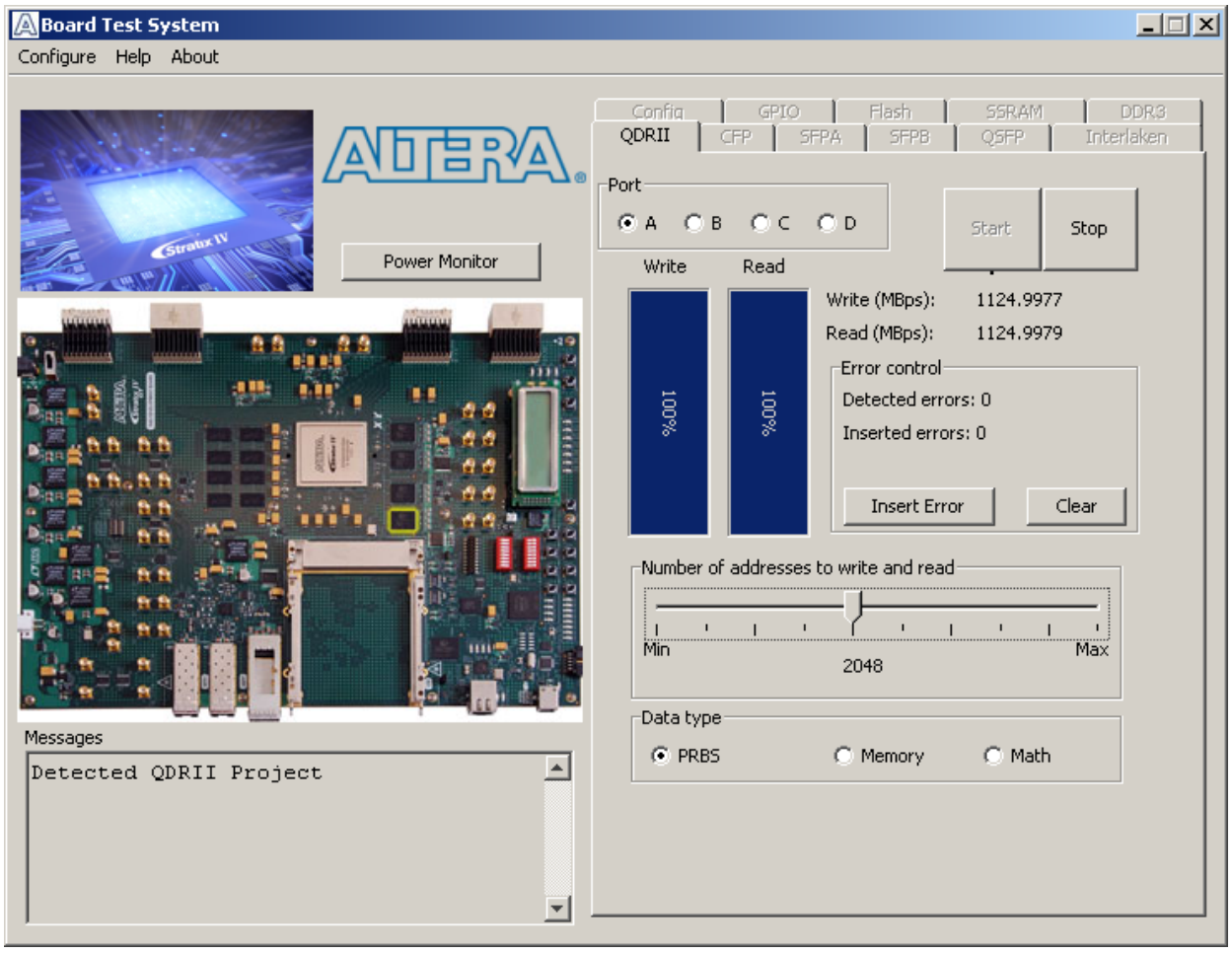
Specifies the type of transactions to analyze. The following transaction types are available for analysis:

- **Write then read**—Selects read and write transactions for analysis.
- **Read only**—Selects read transactions for analysis.
- **Write only**—Selects write transactions for analysis.

The QDRII Tab

The **QDRII** tab allows you to independently test the QDR II interface on your board. Figure 6–8 shows the **QDRII** tab. Since there are four QDR II ports on the Stratix IV GT 100G board, the **QDRII** tab has 4 radio buttons to monitor each QDR II interface.

Figure 6–8. The QDRII Tab



The following sections describe the controls on the **QDRII** tab.

Port

This control directs communications to one of four QDR II memory ports on the board. Each interface is 18 bits wide.

Start

The **Start** control initiates QDR II memory transaction performance analysis.

Stop

The **Stop** control terminates transaction performance analysis.

Performance Indicators

These controls display current transaction performance analysis information collected since you last clicked **Start**:

- **Write** and **Read** performance bars—Show the percentage of maximum theoretical data rate that the requested transactions are able to achieve.
- **Write (MBps)** and **Read (MBps)**—Show the number of bytes of data analyzed per second. The QDR II buses are is 18 bits wide for both read and write, and the frequency is 250 MHz double data rate (500 Mbps per pin), equating to a theoretical maximum bandwidth of 1125 MBps, and 2250 MBps for simultaneous read and write.

Error Control

The **Error control** controls display data errors detected during analysis and allow you to insert errors:

- **Detected errors**—Displays the number of data errors detected in the hardware.
- **Inserted errors**—Displays the number of errors inserted into the transaction stream.
- **Insert Error**—Inserts a one-word error into the transaction stream each time you click the button. **Insert Error** is only enabled during transaction performance analysis.
- **Clear**—Resets the **Detected errors** and **Inserted errors** counters to zeros.

Number of Addresses to Write and Read

The **Number of addresses to write and read** control determines the number of addresses to use in each iteration of reads and writes. Valid values range from 8 to 2,097,152.

Data Type

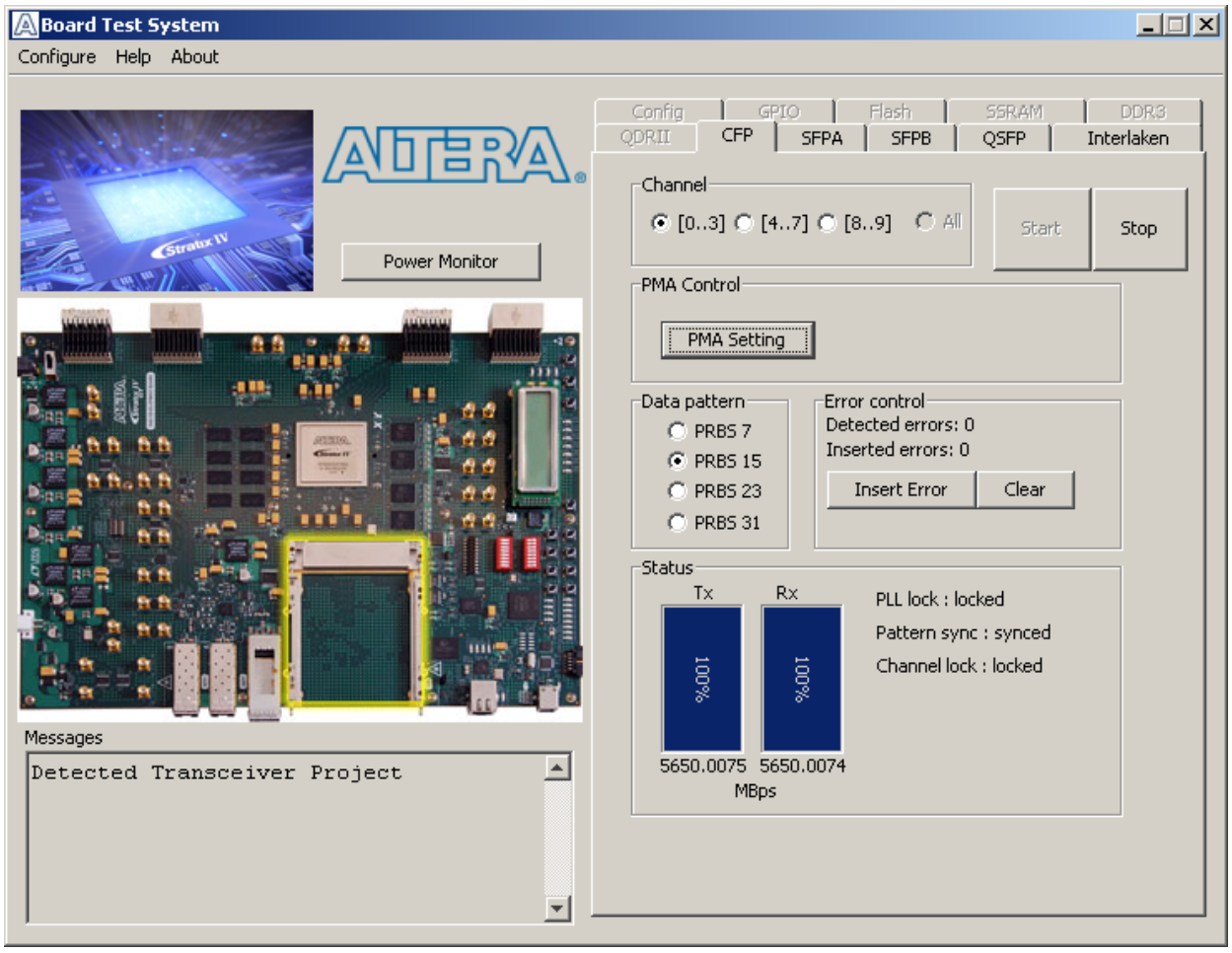
The Data type control specifies the type of data contained in the transactions. The following data types are available for analysis:

- **PRBS**—Selects pseudo-random bit sequences.
- **Memory**—Selects a generic data pattern stored in the on chip memory of the Stratix IV GT device.
- **Math**—Selects data generated from a simple math function within the FPGA fabric.

The CFP Tab

The **CFP** tab allows you to do loopback testing on this interface using different data patterns, PMA settings, and clock speeds using the Clock Control application. Figure 6–9 shows the **CFP** tab.

Figure 6–9. The CFP Tab



You must have the CFP loopback board installed on your 100G development board for this test to work correctly.

The CFP loopback board can be plugged into the connector in either direction. On SIDE A, the transceiver channels go through a retimer device and loops these channels back internally to the FPGA. On SIDE B, the transceiver channels go directly from the receiver to the transmitter without any help from the retimer device. For both sides you need to connect the two SMA connectors with SMA cables. For example, for SIDE A, connect a SMA cable between J6 and J7 and between J9 and J10. For SIDE B, connect a SMA cable between J1 and J5 and J2 and J6.

For more information on the CFP loopback board, refer to the user guide located in the following directory:
*<install dir>***kits\stratixIVGT_4sgt100g5_100g\board_design_files\cfp_loopback\user_guide**.

The following sections describe the controls on the **CFP** tab.

Channel

The **Channel** control allows you to specify channel groups or all channels for analysis.

Start

The **Start** control initiates the loopback tests.

Stop

The **Stop** control terminates the loopback tests.

PMA Setting

The **PMA Setting** button allows you to make changes to the PMA parameters that affect the active transceiver interface. The following settings are available for analysis:

- **Serial Loopback**—Routes signals from the receiver to the transmitter.
- **VOD**—Specifies the voltage output differential of the transmitter buffer.
- **Pre-emphasis tap**
  - **Pre**—Specifies the amount of pre-emphasis on the pre-tap of the transmitter buffer.
  - **First post**—Specifies the amount of pre-emphasis on the first post tap of the transmitter buffer.
  - **Second post**—Specifies the amount of pre-emphasis on the second post tap of the transmitter buffer.
- **Equalizer**—Specifies the setting for the receiver equalizer.
- **DC gain**—Specifies the boost to incoming signals.

Data Pattern

The **Data pattern** control specifies the type of data contained in the transactions. The following data types are available for analysis:

- **PRBS 7**—Selects pseudo-random 7-bit sequences (default.)
- **PRBS 15**—Selects pseudo-random 15-bit sequences.
- **PRBS 23**—Selects pseudo-random 23-bit sequences.
- **PRBS 31**—Selects pseudo-random 31-bit sequences.

Error Control

The **Error control** controls display data errors detected during analysis and allow you to insert errors:

- **Detected errors**—Displays the number of data errors detected in the hardware.
- **Inserted errors**—Displays the number of errors inserted into the transaction stream.
- **Insert Error**—Inserts a one-word error into the transaction stream each time you click the button. **Insert Error** is only enabled during transaction performance analysis.
- **Clear Errors**—Resets the **Detected errors** and **Inserted errors** counters to zeros.

Status

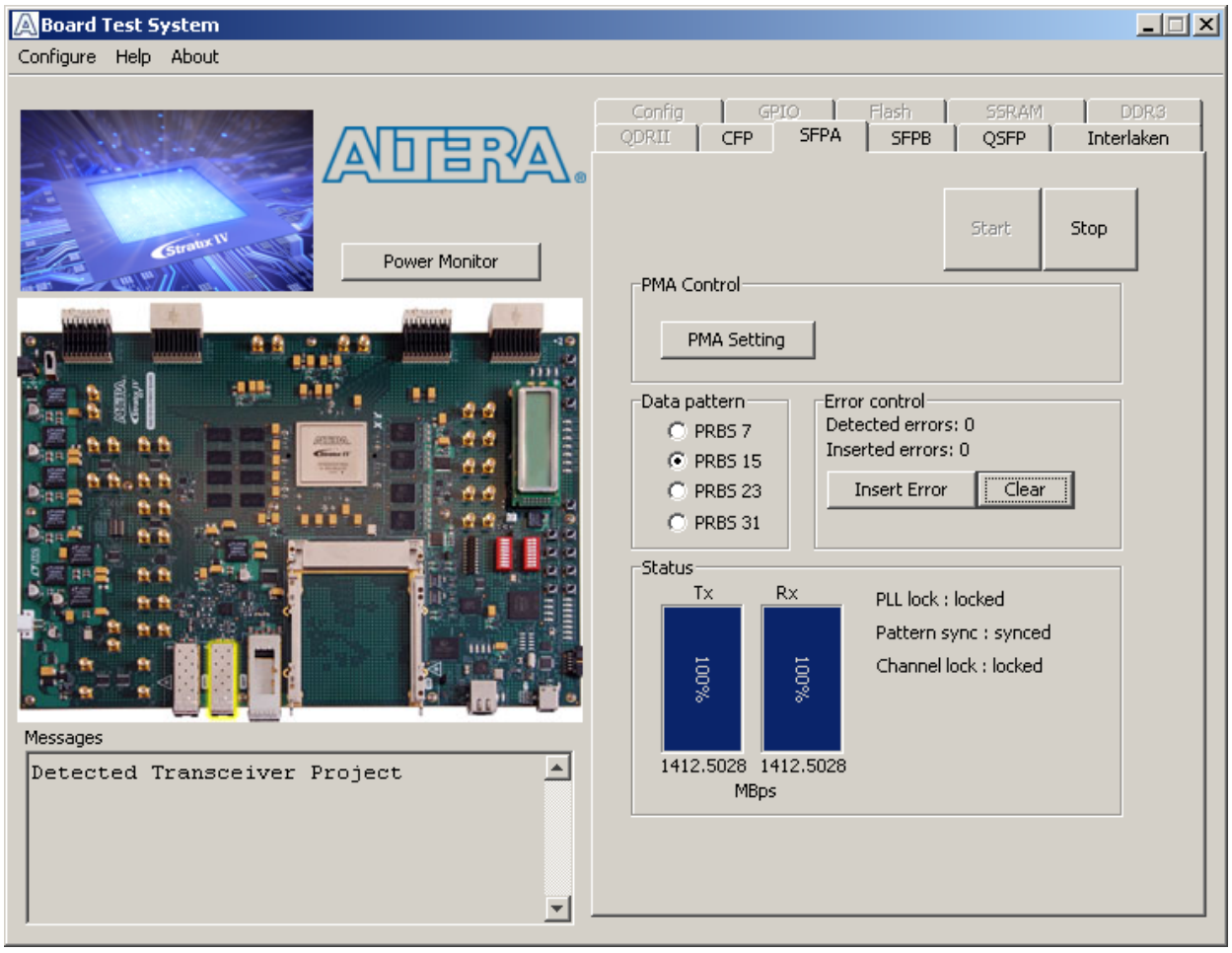
These controls display current transaction performance analysis information collected since you last clicked **Start**:

- **PLL lock**—Shows the PLL locked or unlocked state.
- **Pattern sync**—Shows the pattern synced or not synced state. The pattern is considered synced when the start of the data sequence is detected.
- **TX** and **RX** performance bars—Show the percentage of maximum theoretical data rate that the requested transactions are able to achieve.
- **TX and RX performance**—Shows throughput in decimal form.
- **MBps**—Shows the number of megabytes of data analyzed per second for transmit and receive.

The SFPA Tab

The **SFPA** tab allows you to do loopback testing on this interface using different data patterns, PMA settings, and clock speeds using the Clock Control application. Figure 6–10 shows the **SFPA** tab.

Figure 6–10. The SFPA Tab



You must have the SFPA loopback module installed on your 100G development board for this test to work correctly.

The following sections describe the controls on the **SFPA** tab.

Start

The **Start** control initiates the SFPA loopback test.

Stop

The **Stop** control terminates the SFPA loopback test.

PMA Setting

The **PMA Setting** button allows you to make changes to the PMA parameters that affect the active transceiver interface. The following settings are available for analysis:

- **Serial Loopback**—Routes signals from the receiver to the transmitter.
- **VOD**—Specifies the voltage output differential of the transmitter buffer.
- **Pre-emphasis tap**
  - **Pre**—Specifies the amount of pre-emphasis on the pre-tap of the transmitter buffer.
  - **First post**—Specifies the amount of pre-emphasis on the first post tap of the transmitter buffer.
  - **Second post**—Specifies the amount of pre-emphasis on the second post tap of the transmitter buffer.
- **Equalizer**—Specifies the setting for the receiver equalizer.
- **DC gain**—Specifies the boost to incoming signals.

Data Pattern

The **Data pattern** control specifies the type of data contained in the transactions. The following data types are available for analysis:

- **PRBS 7**—Selects pseudo-random 7-bit sequences.
- **PRBS 15**—Selects pseudo-random 15-bit sequences.
- **PRBS 23**—Selects pseudo-random 23-bit sequences.
- **PRBS 31**—Selects pseudo-random 31-bit sequences.

Error Control

The **Error control** controls display data errors detected during analysis and allow you to insert errors:

- **Detected errors**—Displays the number of data errors detected in the hardware.
- **Inserted errors**—Displays the number of errors inserted into the transaction stream.
- **Insert Error**—Inserts a one-word error into the transaction stream each time you click the button. **Insert Error** is only enabled during transaction performance analysis.
- **Clear**—Resets the **Detected errors** and **Inserted errors** counters to zeros.

Status

These controls display current transaction performance analysis information collected since you last clicked **Start**:

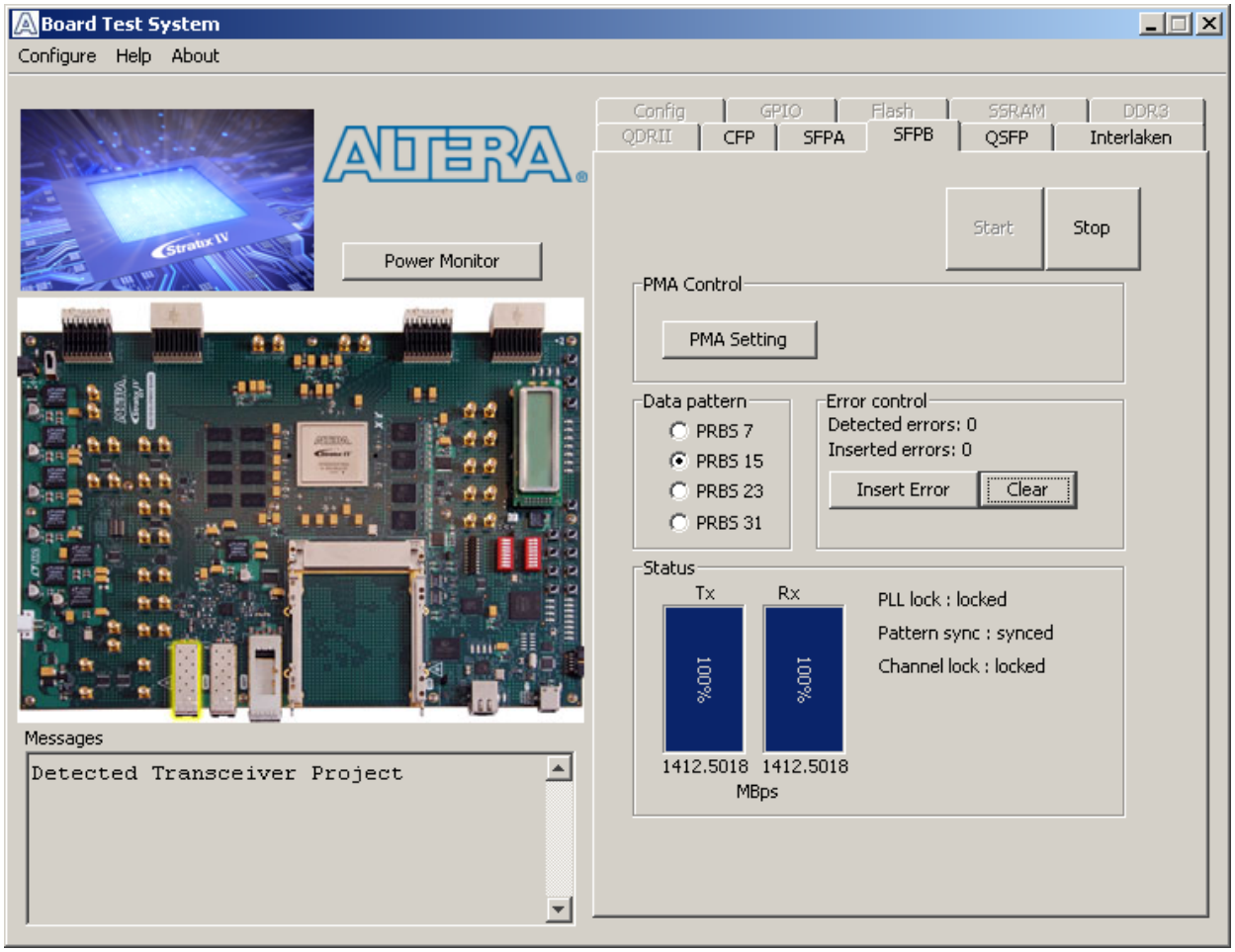
- **PLL lock**—Shows the PLL locked or unlocked state.
- **Pattern sync**—Shows the pattern synced or not synced state. The pattern is considered synced when the start of the data sequence is detected.

- **TX** and **RX** performance bars—Show the percentage of maximum theoretical data rate that the requested transactions are able to achieve.
- **MBps**—Shows the number of megabytes of data analyzed per second for transmit and receive.

The SFPB Tab

The **SFPB** tab allows you to do loopback testing on this interface using different data patterns, PMA settings, and clock speeds using the Clock Control application. Figure 6–11 shows the **SFPB** tab.

Figure 6–11. The SFPB Tab



You must have the SFPB loopback module installed on your 100G development board for this test to work correctly.

The following sections describe the controls on the **SFPB** tab.

Start

The **Start** control initiates the SFPB loopback test.

Stop

The **Stop** control terminates the SFPB loopback test.

PMA Setting

The **PMA Setting** button allows you to make changes to the PMA parameters that affect the active transceiver interface. The following settings are available for analysis:

- **Serial Loopback**—Routes signals from the receiver to the transmitter.
- **VOD**—Specifies the voltage output differential of the transmitter buffer.
- **Pre-emphasis tap**
  - **Pre**—Specifies the amount of pre-emphasis on the pre-tap of the transmitter buffer.
  - **First post**—Specifies the amount of pre-emphasis on the first post tap of the transmitter buffer.
  - **Second post**—Specifies the amount of pre-emphasis on the second post tap of the transmitter buffer.
- **Equalizer**—Specifies the setting for the receiver equalizer.
- **DC gain**—Specifies the boost to incoming signals.
- **Equalizer**—Specifies the setting for the receiver equalizer.
- **DC gain**—Specifies the boost to incoming signals.

Data Pattern

The **Data pattern** control specifies the type of data contained in the transactions. The following data types are available for analysis:

- **PRBS 7**—Selects pseudo-random 7-bit sequences.
- **PRBS 15**—Selects pseudo-random 15-bit sequences.
- **PRBS 23**—Selects pseudo-random 23-bit sequences.
- **PRBS 31**—Selects pseudo-random 31-bit sequences.

Error Control

The **Error control** controls display data errors detected during analysis and allow you to insert errors:

- **Detected errors**—Displays the number of data errors detected in the hardware.
- **Inserted errors**—Displays the number of errors inserted into the transaction stream.
- **Insert Error**—Inserts a one-word error into the transaction stream each time you click the button. **Insert Error** is only enabled during transaction performance analysis.
- **Clear**—Resets the **Detected errors** and **Inserted errors** counters to zeros.

Status

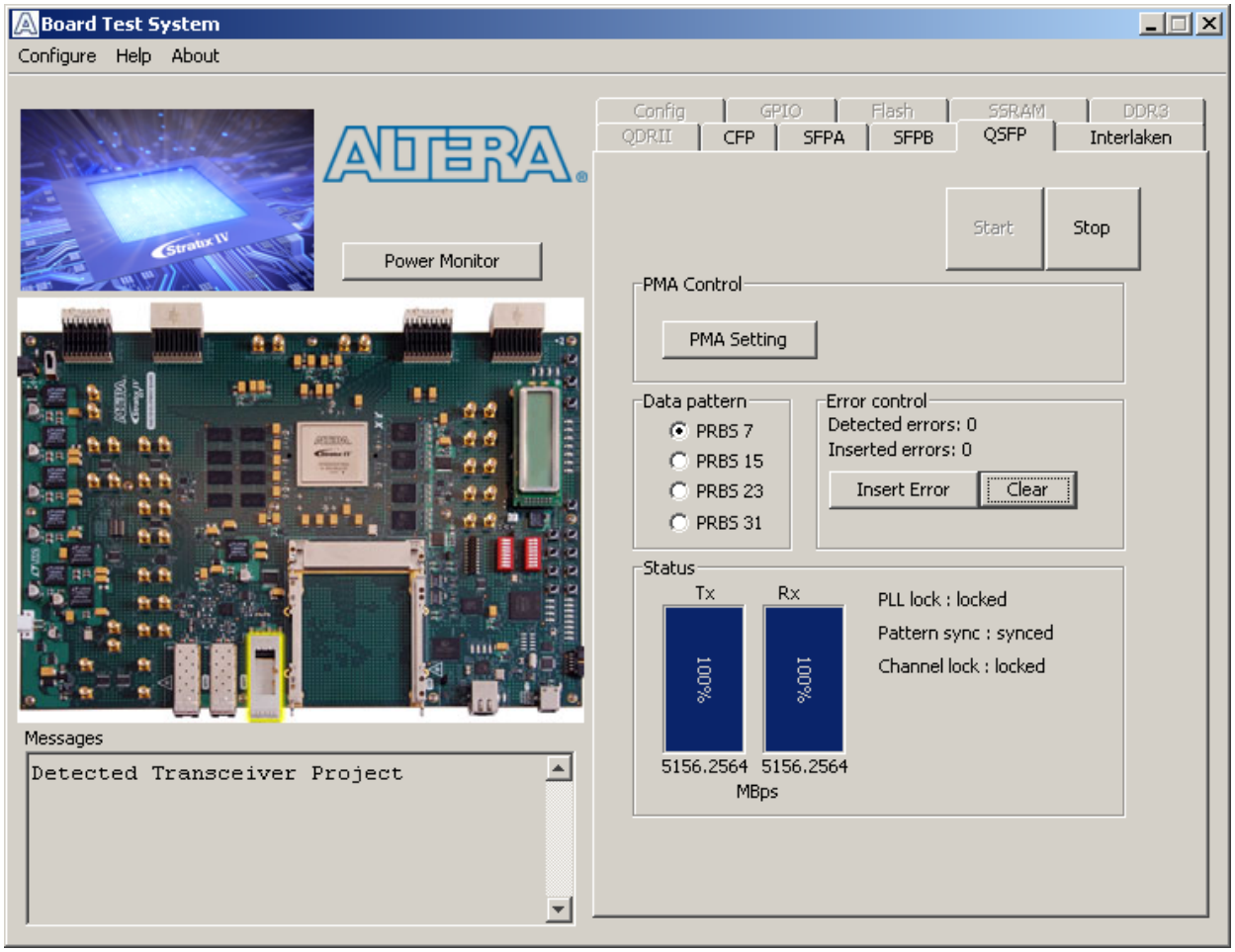
These controls display current transaction performance analysis information collected since you last clicked **Start**:

- **PLL lock**—Shows the PLL locked or unlocked state.
- **Pattern sync**—Shows the pattern synced or not synced state. The pattern is considered synced when the start of the data sequence is detected.
- **TX** and **RX** performance bars—Show the percentage of maximum theoretical data rate that the requested transactions are able to achieve.
- **MBps**—Shows the number of megabytes of data analyzed per second for transmit and receive.

The QSFP Tab

The **QSFP** tab allows you to do loopback testing on this interface using different data patterns, PMA settings, and clock speeds using the Clock Control application. Figure 6–12 shows the **QSFP** tab.

Figure 6–12. The QSFP Tab



You must have the QSFP loopback module installed on your 100G development board for this test to work correctly.

The following sections describe the controls on the **QSFP** tab.

Start

The **Start** control initiates the QSFP loopback test.

Stop

The **Stop** control terminates the QSFP loopback text.

PMA Setting

The **PMA Setting** button allows you to make changes to the PMA parameters that affect the active transceiver interface. The following settings are available for analysis:

- **Serial Loopback**—Routes signals from the receiver to the transmitter.
- **VOD**—Specifies the voltage output differential of the transmitter buffer.
- **Pre-emphasis tap**
  - **Pre**—Specifies the amount of pre-emphasis on the pre-tap of the transmitter buffer.
  - **First post**—Specifies the amount of pre-emphasis on the first post tap of the transmitter buffer.
  - **Second post**—Specifies the amount of pre-emphasis on the second post tap of the transmitter buffer.
- **Equalizer**—Specifies the setting for the receiver equalizer.
- **DC gain**—Specifies the boost to incoming signals.

Data Pattern

The **Data pattern** control specifies the type of data contained in the transactions. The following data types are available for analysis:

- **PRBS 7**—Selects pseudo-random 7-bit sequences.
- **PRBS 15**—Selects pseudo-random 15-bit sequences.
- **PRBS 23**—Selects pseudo-random 23-bit sequences.
- **PRBS 31**—Selects pseudo-random 31-bit sequences.

Error Control

The **Error control** controls display data errors detected during analysis and allow you to insert errors:

- **Detected errors**—Displays the number of data errors detected in the hardware.
- **Inserted errors**—Displays the number of errors inserted into the transaction stream.

- **Insert Error**—Inserts a one-word error into the transaction stream each time you click the button. **Insert Error** is only enabled during transaction performance analysis.
- **Clear**—Resets the **Detected errors** and **Inserted errors** counters to zeros.

Status

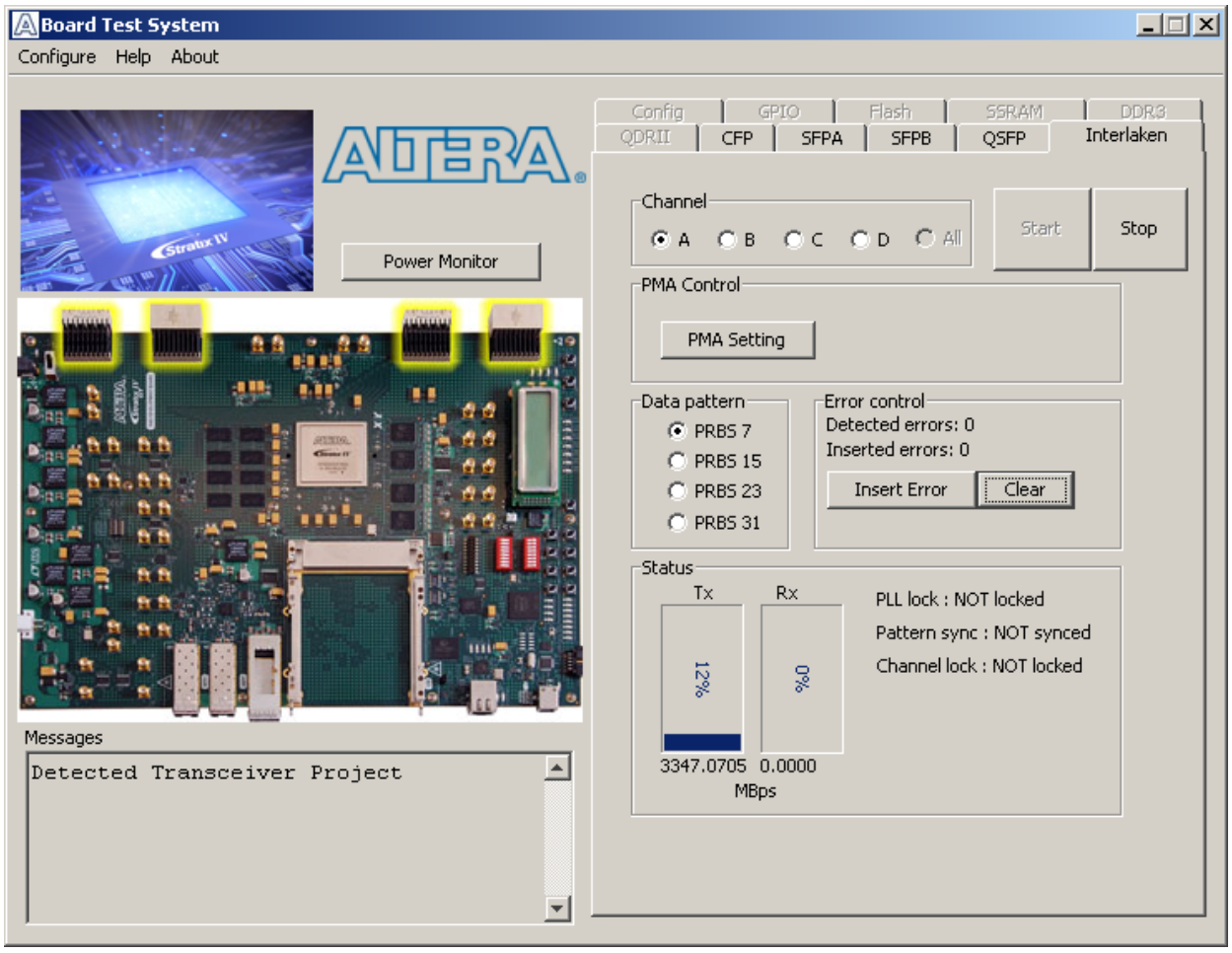
These controls display current transaction performance analysis information collected since you last clicked **Start**:

- **PLL lock**—Shows the PLL locked or unlocked state.
- **Pattern sync**—Shows the pattern synced or not synced state. The pattern is considered synced when the start of the data sequence is detected.
- **TX** and **RX** performance bars—Show the percentage of maximum theoretical data rate that the requested transactions are able to achieve.
- **MBps**—Shows the number of megabytes of data analyzed per second for transmit and receive.

Interlaken Tab

The **Interlaken** tab allows you to do loopback testing on this interface using different data patterns, PMA settings, and clock speeds using the Clock Control application. Figure 6–13 shows the **Interlaken** tab.

Figure 6–13. The Interlaken Tab



You must have both Interlacken loopback cards installed on your 100G development board for this test to work correctly.

The following sections describe the controls on the **Interlaken** tab.

Start

The **Start** control initiates the Interlaken loopback test.

Stop

The **Stop** control terminates the Interlaken loopback test.

PMA Setting

The **PMA Setting** button allows you to make changes to the PMA parameters that affect the active transceiver interface. The following settings are available for analysis:

- **Serial Loopback**—Routes signals from the receiver to the transmitter.
- **VOD**—Specifies the voltage output differential of the transmitter buffer.
- **Pre-emphasis tap**
  - **Pre**—Specifies the amount of pre-emphasis on the pre-tap of the transmitter buffer.
  - **First post**—Specifies the amount of pre-emphasis on the first post tap of the transmitter buffer.
  - **Second post**—Specifies the amount of pre-emphasis on the second post tap of the transmitter buffer.
- **Equalizer**—Specifies the setting for the receiver equalizer.
- **DC gain**—Specifies the boost to incoming signals.

Data Pattern

The **Data pattern** control specifies the type of data contained in the transactions. The following data types are available for analysis:

- **PRBS 7**—Selects pseudo-random 7-bit sequences.
- **PRBS 15**—Selects pseudo-random 15-bit sequences.
- **PRBS 23**—Selects pseudo-random 23-bit sequences.
- **PRBS 31**—Selects pseudo-random 31-bit sequences.

Error Control

The **Error control** controls display data errors detected during analysis and allow you to insert errors:

- **Detected errors**—Displays the number of data errors detected in the hardware.
- **Inserted errors**—Displays the number of errors inserted into the transaction stream.
- **Insert Error**—Inserts a one-word error into the transaction stream each time you click the button. **Insert Error** is only enabled during transaction performance analysis.
- **Clear**—Resets the **Detected errors** and **Inserted errors** counters to zeros.

Status

These controls display current transaction performance analysis information collected since you last clicked **Start**:

- **PLL lock**—Shows the PLL locked or unlocked state.
- **Pattern sync**—Shows the pattern synced or not synced state. The pattern is considered synced when the start of the data sequence is detected.

- **TX** and **RX** performance bars—Show the percentage of maximum theoretical data rate that the requested transactions are able to achieve.
- **MBps**—Shows the number of megabytes of data analyzed per second for transmit and receive.

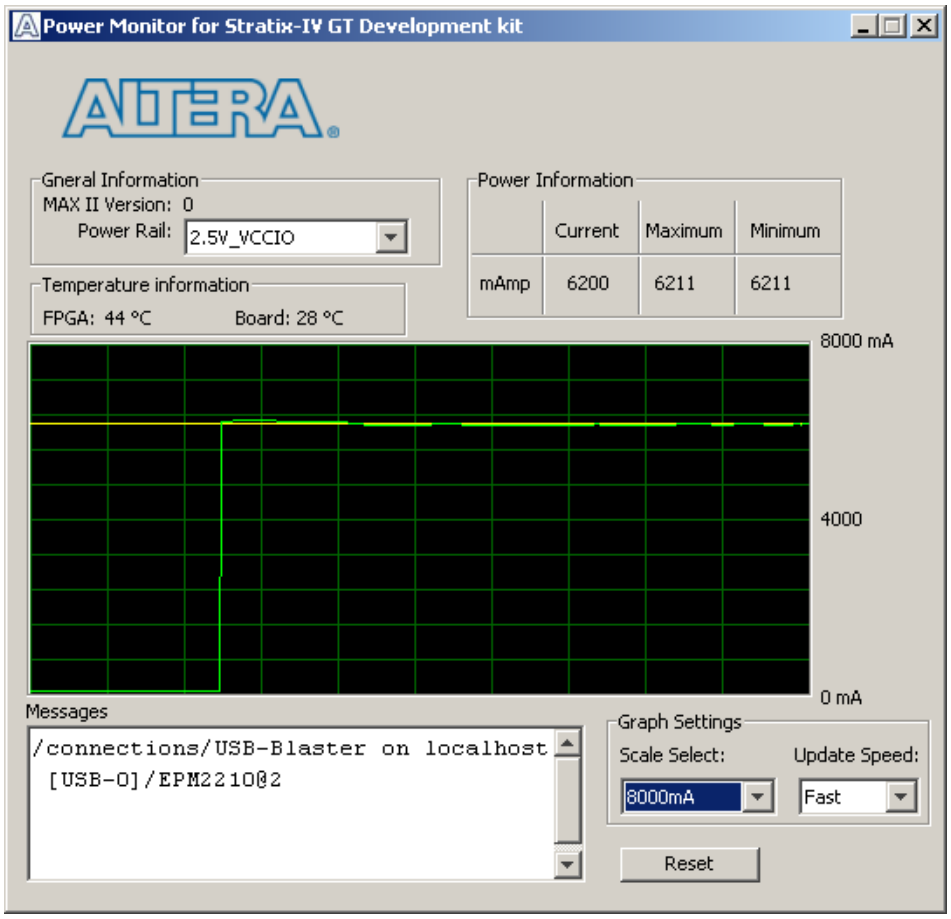
The Power Monitor

The Power Monitor measures and reports current power information for the board. To start the application, click **Power Monitor** in the Board Test System application.

You can also run the Power Monitor as a stand-alone application. **PowerMonitor.exe** resides in the *<install dir>***kits\stratixIVGT_4sgt100g5_100g\examples\board_test_system** directory. On Windows, click **Start** > **All Programs** > **Altera** > **Stratix IV GT 100G Development Kit** *<version>* > **Power Monitor** to start the application.

The Power Monitor communicates with the MAX II device on the board through the JTAG bus. A power monitor circuit attached to the MAX II device allows you to measure the power that the Stratix IV GT FPGA device is consuming regardless of the design currently running. Figure 6–14 shows the Power Monitor.

Figure 6–14. The Power Monitor



The following sections describe the Power Monitor controls.

General Information

The **General information** controls display the following information about the MAX II device:

- **MAX II version**—Indicates the version of MAX II code currently running on the board. The MAX II code resides in the *<install dir>***\kits\stratixIVGT_4sgt100g5_100g\factory_recovery** and *<install dir>***\kits\stratixIVGT_4sgt100g5_100g\examples\max2** directories. Newer revisions of this code might be available on the Stratix IV GT 100G Development Kit page of the Altera website.
- **Power rail**—Selects the power rail to measure. After selecting the desired rail, click **Reset** to refresh the screen with new board readings.

The **Temperature information** controls display the following temperature readings for the board and the FPGA on the board:

- **FPGA**—Indicates the temperature of the FPGA device.
- **Board**—Indicates the overall board temperature.

Power Information

The **Power information** control displays current, maximum, and minimum power readings for the mAmp unit.

Power Graph

The power graph displays the mAmp current of your board over time. The green line indicates the current value. The red line indicates the maximum value read since the last reset. The yellow line indicates the minimum value read since the last reset.

Graph Settings

The following **Graph settings** controls allow you to define the look and feel of the power graph:

- **Scale select**—Specifies the amount to scale the power graph. Select a smaller number to zoom in to see finer detail. Select a larger number to zoom out to see the entire range of recorded values.
- **Update speed**—Specifies how often to refresh the graph.

Reset

This **Reset** control clears the graph, resets the minimum and maximum values, and restarts the Power Monitor.

Calculating Power

The Power Monitor calculates power by measuring two different voltages with the LT2418 A/D and applying the equation $P = V \times I$ to determine the power consumption. The LT2418 measures the voltage after the appropriate sense resistor (*Vsense*) and the voltage drop across that sense resistor (*Vdif*). The current (*I*) is calculated by dividing the measured voltage drop across the resistor by the value of the sense resistor ($I = Vdif/R$). Through substitution, the equation for calculating power becomes $P = V \times I = Vsense \times (Vdif/R) = (Vsense) \times (Vdif) \times (1/.003)$.

You can verify the power numbers shown in the Power Monitor with a digital multimeter that is capable of measuring microvolts to ensure you have enough significant digits for an accurate calculation. Measure the voltage on one side of the resistor (the side opposite the power source) and then measure the voltage on the other side. The first measurement is *Vsense* and the difference between the two measurements is *Vdif*. Plug the values into the equation to determine the power consumption.

The Clock Control

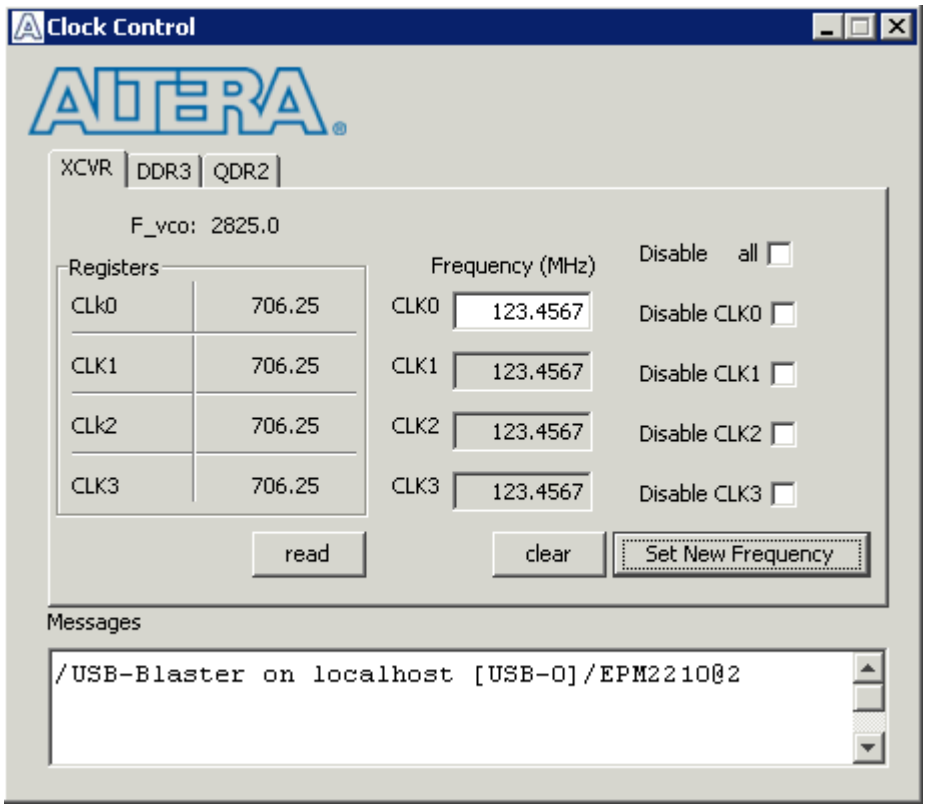
The Clock Control application sets the Si5338 programmable oscillator to any frequency between 0.16 MHz and 710 MHz. Each clock generator device contains a PLL and buffer inside its device that drives four independent LVDS clocks to the FPGA core for the DDR3 and four clocks to the QDRII memory interfaces. There is also a clock generator that drives four independent LVDS clocks to the reference clock inputs for the transceivers. All of these clock generators come pre-programmed with the 100G development board. The memory clocks are pre-programmed to 100 MHz and the transceiver clocks are pre-programmed to 706.25 MHz.

The Clock Control application runs as a stand-alone application. **ClockControl.exe** resides in the <*install dir*>**\kits\stratixIVGT_4sgt100g5_100g\examples\board_test_system** directory. On Windows, click **Start** > **All Programs** > **Altera** > **Stratix IV GT 100G Development Kit** <*version*> > **Clock Control** to start the application.

For more information about the Si5338 and the Stratix IV GT 100G development board's clocking circuitry and clock input pins, refer to the *Stratix IV GT 100G Development Board Reference Manual*.

The Clock Control communicates with the MAX II device on the board through the JTAG bus. The Si5338 programmable oscillator is connected to the MAX II device through a 2-wire serial bus. Figure 6–15 shows the Clock Control application.

Figure 6–15. The Clock Control



The following sections describe the Clock Control controls.

Clock Tabs

There are three tabs to control each clock generator device. The **XCVR** tab controls the clocks to the transceiver reference clock input. The default is 706.25 MHz. The **DDR3** tab controls the clocks for the DDR3 interface. Its default along with the **QDR2** tab is 100 MHz. The **QDR2** tab controls the clocks for the QDRII interface.

Registers

The **Registers** control shows the current values from **the clock driver**.

Frequency

Enter the desired frequencies for each CLK. The range of this GUI is from 5 MHz to 710 MHz. There are some limitations for what frequencies are allowed.

For more information about the Si5338, refer to the datasheet on the Silicon Labs website (www.silabs.com).

Disable ALL

Disables all of the outputs of the clock generator.

Read

Reads the register values and calculates the frequency based on these values.

Clear

Resets the device and puts it back in the factory default state.

Set New Frequency

The **Set New Frequency** control sets the desired frequency after this button is pressed.

Configuring the FPGA Using the Quartus II Programmer

You can use the Quartus II Programmer to configure the FPGA with a specific SRAM Object File (**.sof)**. Before configuring the FPGA, ensure that the Quartus II Programmer and the USB-Blaster driver are installed on the host computer, the USB cable is connected to the 100G development board, power to the board is on, and no other applications that use the JTAG chain are running.

To configure the Stratix IV GT FPGA, perform the following steps:

1. Start the Quartus II Programmer.
2. Click **Add File** and select the path to the desired **.sof**.
3. Turn on the **Program/Configure** option for the added file.
4. Click **Start** to download the selected file to the FPGA. Configuration is complete when the progress bar reaches 100%.

Using the Quartus II programmer to configure a device on the board causes other JTAG-based applications such as the Board Test System and the Power Monitor to loose their connection to the board. Restart those applications after configuration is complete.

A. Programming the Flash Memory Device

As you develop your own project using the Altera tools, you can program the flash memory device so that your own design loads from flash memory into the FPGA on power up. This appendix describes the preprogrammed contents of the common flash interface (CFI) flash memory device on the Stratix IV GT 100G development board and the Nios II EDS tools involved with reprogramming the user portions of the flash memory device.

The Stratix IV GT 100G development board ships with the CFI flash device preprogrammed with a default factory FPGA configuration for running the Board Update Portal design example and a default user configuration for running the Board Test System demonstration. There are several other factory software files written to the CFI flash device to support the Board Update Portal. These software files were created using the Nios II EDS, just as the hardware design was created using the Quartus II software.

For more information about Altera development tools, refer to the Design Software page of the Altera website.

CFI Flash Memory Map

Table A–1 shows the default memory contents of the 128-Mb (1-Gbit) single-die CFI flash device. For the Board Update Portal to run correctly and update designs in the user memory, this memory map must not be altered.

Table A–1. Byte Address Flash Memory Map

Block Description	Size	Address Range
Unused	128 KB	0x07FE0000 - 0x07FFFFFF
User software	26,624 KB	0x065E0000 - 0x07FDFFFF
Factory software	4,096 KB	0x061E0000 - 0x065DFFFF
zipfs (html, web content)	4,096 KB	0x05DE0000 - 0x061DFFFF
User hardware 3	21, 116 KB	0x04940000 - 0x05DDFFFF
User hardware 2	21, 116 KB	0x034A0000 - 0x0493FFFF
User hardware 1	21, 116 KB	0x02000000 - 0x0349FFFF
Reserved	11,136 KB	0x01520000 - 0x01FFFFFF
Factory hardware	21, 116 KB	0x00080000 - 0x0151FFFF
PFL option bits	128 KB	0x00060000 - 0x0007FFFF
Board information	128 KB	0x00040000 - 0x0005FFFF
Ethernet option bits	128 KB	0x00020000 - 0x0003FFFF
User design reset vector	128 KB	0x00000000 - 0x0001FFFF

CAUTION

Altera recommends that you do not overwrite the factory hardware and factory software images unless you are an expert with the Altera tools. If you unintentionally overwrite the factory hardware or factory software image, refer to "Restoring the Flash Device to the Factory Settings" on page A–4.

Preparing Design Files for Flash Programming

You can obtain designs containing prepared **.flash** files from the Stratix IV GT 100G Development Kit page of the Altera website or create **.flash** files from your own custom design.

The Nios II EDS **sof2flash** command line utility converts your Quartus II-compiled **.sof** into the **.flash** format necessary for the flash device. Similarly, the Nios II EDS **elf2flash** command line utility converts your compiled and linked Executable and Linking Format File (**.elf**) software design to **.flash**. After your design files are in the **.flash** format, use the Board Update Portal or the Nios II EDS **nios2-flash-programmer** utility to write the **.flash** files to the user hardware and user software locations of the flash memory.

For more information about Nios II EDS software tools and practices, refer to the Embedded Software Development page of the Altera website.

Creating Flash Files Using the Nios II EDS

If you have an FPGA design developed using the Quartus II software, and software developed using the Nios II EDS, follow these instructions:

1. On the Windows Start menu, click **All Programs** > **Altera** > **Nios II EDS** > **Nios II Command Shell**.
2. In the Nios II command shell, navigate to the directory where your design files reside and type the following Nios II EDS commands:
   - For Quartus II **.sof** files:

```
sof2flash --input=<yourfile>_hw.sof --output=<yourfile>_hw.flash --offset=0x2000000
--pfl --optionbit=0x00060000 --programmingmode=PS↵
```

   - For Nios II **.elf** files:

```
elf2flash --base=0x08000000 --end=0xFFFFFFF --reset=0x0E5E0000
--input=<yourfile>_sw.elf --output=<yourfile>_sw.flash
--boot=$SOPC_KIT_NIOS2/components/altera_nios2/
  boot_loader_sources/boot_loader_cfi.srec↵
```

The resulting **.flash** files are ready for flash device programming. If your design uses additional files such as image data or files used by the runtime program, you must first convert the files to **.flash** format and concatenate them into one **.flash** file before using the Board Update Portal to upload them.

The Board Update Portal standard **.flash** format conventionally uses either <*filename*>**_hw.flash** for hardware design files or <*filename*>**_sw.flash** for software design files.

Programming Flash Memory Using the Board Update Portal

Once you have the necessary **.flash** files, you can use the Board Update Portal to reprogram the flash memory. Refer to "Using the Board Update Portal to Update User Designs" on page 5–2 for more information.

If you have generated a **.sof** that operates without a software design file, you can still use the Board Update Portal to upload your design. In this case, leave the **Software File Name** field blank.

Programming Flash Memory Using the Nios II EDS

The Nios II EDS offers a **nios2-flash-programmer** utility to program the flash memory directly. To program the **.flash** files or any compatible S-Record File (**.srec**) to the board using **nios2-flash-programmer**, perform the following steps:

1. Attach the USB-Blaster cable and power up the board.
2. Press FACTORY (S12) to load the Board Update Portal design from flash memory.
3. If the board has configured and the LCD displays either "Connecting..." or a valid IP address (such as 152.198.231.75), proceed to step 8. If no output appears on the LCD or if the MAX_CONF (D37) does not illuminate, continue to step 4 to load the FPGA with a flash-writing design.
4. Launch the Quartus II Programmer to configure the FPGA with a **.sof** capable of flash programming. Refer to "Configuring the FPGA Using the Quartus II Programmer" on page 6–33 for more information.
5. Click **Add File** and select *<install dir>***\kits\stratixIVGT_4sgt100g5_100g\factory_recovery\s4gt100g_fpga_bup.sof**.
6. Turn on the **Program/Configure** option for the added file.
7. Click **Start** to download the selected configuration file to the FPGA. Configuration is complete when the progress bar reaches 100%. The MAX_CONF (D37) and the user LEDs (D28-D35) illuminate indicating that the flash device is ready for programming.
8. On the Windows Start menu, click **All Programs** > **Altera** > **Nios II EDS** > **Nios II Command Shell**.
9. In the Nios II command shell, navigate to the *<install dir>***\kits\stratixIVGT_4sgt100g5_100g\factory_recovery** directory (or to the directory of the **.flash** files you created in "Creating Flash Files Using the Nios II EDS" on page A–2) and type the following Nios II EDS command:

```
nios2-flash-programmer --base=0x08000000 <yourfile>_hw.flash ↵
```

10. After programming completes, if you have a software file to program, type the following Nios II EDS command:

```
nios2-flash-programmer --base=0x08000000 <yourfile>_sw.flash ↵
```

11. Press PGM_SEL (S10) until the USER POF LED 1 (D19) illuminates; then press LOAD (S11) to load and run the user design.

Programming the board is now complete.

For more information about the **nios2-flash-programmer** utility, refer to the *Nios II Flash Programmer User Guide*.

Restoring the Flash Device to the Factory Settings

This section describes how to restore the original factory contents to the flash memory device on the 100G development board. Make sure you have the Nios II EDS installed, and perform the following instructions:

1. Set the board switches to the factory default settings described in "Factory Default Switch Settings" on page 4–2.
2. Launch the Quartus II Programmer to configure the FPGA with a **.sof** capable of flash programming. Refer to "Configuring the FPGA Using the Quartus II Programmer" on page 6–33 for more information.
3. Click **Add File** and select *<install dir>***\kits\stratixIVGT_4sgt100g5_100g\factory_recovery\s4gt100g_fpga_bup.sof**.
4. Turn on the **Program/Configure** option for the added file.
5. Click **Start** to download the selected configuration file to the FPGA. Configuration is complete when the progress bar reaches 100%. The MAX_CONF (D37) and the user LEDs (D28-D35) illuminate indicating that the flash device is ready for programming.
6. On the Windows Start menu, click **All Programs** > **Altera** > **Nios II EDS** > **Nios II Command Shell**.
7. In the Nios II command shell, navigate to the *<install dir>***\kits\stratixIVGT_4sgt100g5_100g\factory_recovery** directory and type the following command to run the restore script:

   ```
   ./restore.sh ↵
   ```

   Restoring the flash memory might take several minutes. Follow any instructions that appear in the Nios II command shell.
8. After all flash programming completes, cycle the POWER switch (SW1) off then on.
9. Using the Quartus II Programmer, click **Add File** and select *<install dir>***\kits\stratixIVGT_4sgt100g5_100g\factory_recovery\s4gt100g_fpga_bup.sof**.
10. Turn on the **Program/Configure** option for the added file.
11. Click **Start** to download the selected configuration file to the FPGA. Configuration is complete when the progress bar reaches 100%. The MAX_CONF (D37) and the user LEDs (D28-D35) illuminate indicating the flash memory device is now restored with the factory contents.
12. Press FACTORY (S12) to load the Board Update Portal design from flash memory.

13. The restore script cannot restore the board's MAC address automatically. In the Nios II command shell, type the following Nios II EDS command:

    ```
    nios2-terminal ↵
    ```

    and follow the instructions in the terminal window to generate a unique MAC address.

To ensure that you have the most up-to-date factory restore files and information about this product, refer to the Stratix IV GT 100G Development Kit page of the Altera website.

Restoring the MAX II CPLD to the Factory Settings

This section describes how to restore the original factory contents to the MAX II CPLD on the 100G development board. Make sure you have the Nios II EDS installed, and perform the following instructions:

1. Set the board switches to the factory default settings described in "Factory Default Switch Settings" on page 4–2.

   The installed jumper for JTAG_EN (J41) includes the MAX II device in the JTAG chain.

2. Launch the Quartus II Programmer.
3. Click **Auto Detect**.
4. Click **Add File** and select *<install dir>***kits\stratixIVGT_4sgt100g5_100g\factory_recovery\max2.pof**.
5. Turn on the **Program/Configure** option for the added file.
6. Click **Start** to download the selected configuration file to the MAX II CPLD. Configuration is complete when the progress bar reaches 100%.

To ensure that you have the most up-to-date factory restore files and information about this product, refer to the Stratix IV GT 100G Development Kit page of the Altera website.

This chapter provides additional information about the document and Altera.

Document Revision History

The following table shows the revision history for this document.

Date	Version	Changes
Oct. 14, 2010	1.1	Corrected elf2flash addresses.
Sep. 23, 2010	1.0	Initial release.

How to Contact Altera

To locate the most up-to-date information about Altera products, refer to the following table.

Contact *(1)*	Contact Method	Address
Technical support	Website	www.altera.com/support
Technical training	Website	www.altera.com/training
	Email	custrain@altera.com
Product literature	Website	www.altera.com/literature
Non-technical support (General)	Email	nacomp@altera.com
(Software Licensing)	Email	authorization@altera.com

Note to Table:

(1) You can also contact your local Altera sales office or sales representative.

Typographic Conventions

The following table shows the typographic conventions this document uses.

Visual Cue	Meaning
Bold Type with Initial Capital Letters	Indicate command names, dialog box titles, dialog box options, and other GUI labels. For example, **Save As** dialog box. For GUI elements, capitalization matches the GUI.
bold type	Indicates directory names, project names, disk drive names, file names, file name extensions, software utility names, and GUI labels. For example, **\qdesigns** directory, **D:** drive, and **chiptrip.gdf** file.
Italic Type with Initial Capital Letters	Indicate document titles. For example, *Stratix IV Design Guidelines*.
italic type	Indicates variables. For example, *n* + 1. Variable names are enclosed in angle brackets (< >). For example, *<file name>* and *<project name>***.pof** file.

Visual Cue	Meaning
Initial Capital Letters	Indicate keyboard keys and menu names. For example, the Delete key and the Options menu.
"Subheading Title"	Quotation marks indicate references to sections within a document and titles of Quartus II Help topics. For example, "Typographic Conventions."
`Courier type`	Indicates signal, port, register, bit, block, and primitive names. For example, `data1`, `tdi`, and `input`. The suffix `n` denotes an active-low signal. For example, `resetn`. Indicates command line commands and anything that must be typed exactly as it appears. For example, `c:\qdesigns\tutorial\chiptrip.gdf`. Also indicates sections of an actual file, such as a Report File, references to parts of files (for example, the AHDL keyword `SUBDESIGN`), and logic function names (for example, `TRI`).
↵	An angled arrow instructs you to press the Enter key.
1., 2., 3., and a., b., c., and so on	Numbered steps indicate a list of items when the sequence of the items is important, such as the steps listed in a procedure.
■ ■ ■	Bullets indicate a list of items when the sequence of the items is not important.
	The hand points to information that requires special attention.
	A question mark directs you to a software help system with related information.
	The feet direct you to another document or website with related information.
	A caution calls attention to a condition or possible situation that can damage or destroy the product or your work.
	A warning calls attention to a condition or possible situation that can cause you injury.
	The envelope links to the Email Subscription Management Center page of the Altera website, where you can sign up to receive update notifications for Altera documents.